Examples

Table of contents

cuMAC test vectors generated as HDF5 files

Test vectors are located in the `testVectors` directory. Each test vector contains parameters and data arrays defined in the cuMAC API structures (`aerial_sdk/cuMAC/src/api.h`): `cumacCellGrpUeStatus` , `cumacCellGrpPrms` , and `cumacSchdSol` .

Parameter configurations can be specified the `aerial_sdk/cuMAC/examples/parameters.h` file.

Use the multiCellSchedulerUeSelection testbench (`aerial_sdk/cuMAC/examples/multiCellSchedulerUeSelection`) to create TVs:

- DL TV:

```
./aerial_sdk/cuMAC/build/examples/multiCellSchedulerUeSelection/multiCellSch
-t 1
```

- UL TV:

```
./aerial_sdk/cuMAC/build/examples/multiCellSchedulerUeSelection/multiCellSch
-d 0 -t 1
```

An H5 TV is created after the last simulated TTI. The assumption is that the simulation duration is long enough so that the scheduler algorithm's performance converges.

Single-TTI tests

Given the same input parameters of a single TTI, GPU and CPU implementations of the same scheduler algorithms should give the same output solution.

Two types of tests:

- Per scheduler module tests: DL/UL UE selection, DL/UL PRG allocation, DL/UL layer selection, and DL/UL MCS selection
- Complete DL/UL scheduler pipeline tests

TV loading-based single-TTI testbench (`aerial_sdk/cuMAC/examples/tvLoadingTest`).

After building cumac, use the following commend to check input arguments of the testbench: `./aerial_sdk/cuMAC/build/examples/tvLoadingTest/tvLoadingTest -h`

- Per scheduler module tests:
    - DL UE selection:

      ```
      ./aerial_sdk/cuMAC/build/examples/tvLoadingTest/tvLoadingTest -i [path to TV] -g 2 -d 1 -m 01000
      ```

    - DL PRG allocation:

      ```
      ./aerial_sdk/cuMAC/build/examples/tvLoadingTest/tvLoadingTest -i [path to TV] -g 2 -d 1 -m 00100
      ```

    - DL layer selection:

      ```
      ./aerial_sdk/cuMAC/build/examples/tvLoadingTest/tvLoadingTest -i [path to TV] -g 2 -d 1 -m 00010
      ```

    - DL MCS selection:

      ```
      ./aerial_sdk/cuMAC/build/examples/tvLoadingTest/tvLoadingTest -i [path to TV] -g 2 -d 1 -m 00001
      ```

    - UL scheduler modules can be tested by setting input argument: `-d 0`
- Complete DL/UL scheduler pipeline tests
    - DL/UL scheduler modules executed sequentially: UE selection > PRG allocation > layer selection > MCS selection
    - DL scheduler pipeline:

```
./aerial_sdk/cuMAC/build/examples/tvLoadingTest/tvLoadingTest -i [path to TV] -g 2 -d 1 -m 01111
```

- UL scheduler pipeline:

```
./aerial_sdk/cuMAC/build/examples/tvLoadingTest/tvLoadingTest -i [path to TV] -g 2 -d 0 -m 01111
```

Passing criteria:

Solutions computed by CPU and GPU should match exactly: testbench returns 1 (PASS) or 0 (FAIL)

Continuous-time tests

With the same initial sate, GPU and CPU implementations of the same scheduler algorithms should achieve similar performance curves when running for a period of time.

- Complete DL/UL scheduler pipeline tests
  - Continuous-time testbench (`aerial_sdk/cuMAC/examples/multiCellSchedulerUeSelection`)
  - After building cumac, use the following commend to check input arguments of the testbench:

```
./aerial_sdk/cuMAC/build/examples/multiCellSchedulerUeSelection/multiCe
-h
```

  - No need to use pre-generated H5 TVs. All parameters are computed using cuMAC internal simulator.
  - Simulator configuration can be specified using the `aerial_sdk/cuMAC/examples/parameters.h` file.
  - DL/UL scheduler modules executed sequentially: UE selection > PRG allocation > layer selection > MCS selection

- DL scheduler pipeline test:

```
./aerial_sdk/cuMAC/build/examples/multiCellSchedulerUeSelection/multiCe
```

- UL scheduler pipeline test:

```
./aerial_sdk/cuMAC/build/examples/multiCellSchedulerUeSelection/multiCe
-d 0
```

Passing criteria:

Performance curves achieved by GPU and CPU scheduler implementations should match: testbench returns 1 (PASS) or 0 (FAIL)

Two types of performance curves:

- Sum throughput of all cells
- CDF of per-UE throughput