



# **BESS Self-Qualification Guidelines**

Application Note



# Document History

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# Introduction

## Use Cases for BESS

The BESS qualification addresses the following primary use cases for grid-interactive battery energy storage at AI data center campuses:

- Low Voltage Ride-Through (LVRT) — Maintain continuous operation during grid voltage disturbances, preventing costly IT load interruptions.
- Dynamic AI Transient Reduction — Buffer rapid power ramps generated by AI workloads to prevent source instability and POI violations.
- Demand Response (DR) — Dispatch stored energy on command to reduce peak grid draw while preserving buffering and ride-through reserves.
- Source Transfer — Enable seamless transitions between grid-connected and islanded operating modes without loss of load.
- Black Start — Energize a de-energized bus and establish stable voltage and frequency to restore site power independently.

This application note defines the partner-run qualification process for a Battery Energy Storage System (BESS) intended to support AI load buffering, demand response (DR), and low voltage ride-through (LVRT) in grid-connected and islanded onsite generation modes.

The goal is to verify the availability and performance of key requirements for a grid-adaptive power conversion system (PCS)-based BESS capable of meeting specified latency and performance targets across grid-connected and islanded operating modes, including: dynamic real/reactive power response, current limiting behavior, ride-through behavior, islanded stability, black start, seamless grid/island transitions, telemetry, and control transparency.

Once the process is complete, all test data must be submitted to NVIDIA for review and approval. Submissions shall include all information necessary and sufficient to demonstrate compliance with each requirement. Any changes to the requirements must be reviewed and approved by the owner's representatives.

# Qualification Boundary

This self-qualification explicitly defines the BESS boundary at the AC terminals (PCS inclusive) because the BESS is being qualified as a grid asset. The qualification addresses PCS performance behavior—a gap no existing standard fills. Site transformers, line reactors, switchgear, relays, generators, and campus control systems are not qualified here. However, the partner must provide models and evidence sufficient for NVIDIA to validate site-level integration.

Passing qualification does not imply site-level stability. However, failure to demonstrate stability across the defined SCR, impedance, and load envelopes constitutes BESS non-qualification regardless of downstream integration.

The following domains are deliberately excluded from this qualification scope, as they fall under OEM responsibility or existing regulatory frameworks.

## Battery Sizing

Battery sizing is irrelevant to qualification. Test 11 (SOC Drift) requires control logic to manage energy balance. Oversizing the battery explicitly does not satisfy this requirement. Any reasonably sized system with well-tuned controls should be able to pass.

## DC Blocks

DC block topology is outside the qualification boundary, which is defined at the AC terminals. Vendors may use a single large DC block or multiple smaller ones but must demonstrate compliance at the point of interconnection (POI).

## Cell Chemistry

Cell chemistry affects energy density, cycle life, and cost—all OEM decisions that are beyond this qualification's scope. The tests (ramp response, current limit, LVRT) are chemistry-agnostic by design. A system passes or fails based on PCS behavior alone.

## Cybersecurity

Cybersecurity requirements for grid-interactive devices, including BESS PCS, are governed by existing frameworks such as NERC CIP, IEC 62443, and NIST CSF. These standards bodies and regulatory bodies already own this domain. NVIDIA applies those requirements broadly to all IoT devices, BESS PCS included, rather than introducing a redundant or potentially inconsistent parallel requirement.

# Safety

Safety requirements—including fire suppression, NFPA 855, UL 9540A, seismic, and related standards—are governed by the Authority Having Jurisdiction (AHJ) and applicable regulatory bodies, not by NVIDIA. NVIDIA is not a safety certification body, and duplicating those requirements here would be redundant and outside the scope of this qualification.

# General Expectations

Partners must follow this guideline exactly. Submissions must be clear, complete, and technically defensible.

Minimum expectations:

- All acronyms defined on first use.
- All tests include raw time-series data at required sampling rates.
- All plots include axis units, ranges, and timestamps.
- Any deviation from requirements requires a written deviation request and proposed mitigation.
- Partner must provide both: (a) Hardware test evidence (bench, HIL, factory test, or field test), and (b) Model evidence (EMT modeling + small-signal) for untestable edge cases.
- If a capability is claimed, it must be demonstrated with data and/or validated models. No marketing claims accepted.
- Submissions shall include all information necessary and sufficient to demonstrate compliance.

# Confidentiality

All materials provided under this qualification process are treated as NVIDIA Confidential and subject to applicable non-disclosure agreements.

- Partners may designate proprietary implementation details (e.g., controller source code, internal firmware) as restricted.
- Measured performance data, test results, and qualification outcomes are not considered proprietary.
- Encrypted or compiled models are acceptable, provided they are runnable and allow modification of external grid and load parameters.
- Claims of confidentiality may not be used to withhold data required to verify compliance.

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# BESS Qualification Overview

This section provides an overview of the qualification process, from product requirements document (PRD) review to partner listing.

## Step 1: Product Requirements Document (PRD) Review

Partner must respond to each PRD requirement line with: Compliant / Non-compliant / Exception (C, D, or E).

- For non-compliance: current behavior, roadmap, workaround, and risk.
- For exceptions: explain the technical substitute and results.
- Reference to specific evidence: test ID, plot, model, or certificate.

Reference document: "BESS Requirements Document"

Table 1. BESS Qualification PRD Response Example

Note: Since the qualification boundary is at BESS AC terminals, "POI ramp" requirements are verified using an approved POI proxy: a commanded P profile equivalent to the required POI shaping, and/or EMT verification using partner-provided models.

Requirement ID	Item	Description	Partner Response
CTRL-REQ-01	Grid-Adaptive Control	PCS shall sustain stable island mode operation, including voltage and frequency control independent of grid synchronization signals	Compliant / Non-compliant / Exception (Reference specific evidence: test ID, plot, model, or certificate)
PERF-REQ-02	Ramp Limit	Demonstrate active ramp-rate smoothing to buffer the source	Compliant. Evidence: Test 4,5 and 11

		from sudden AI load swings. The system must maintain constant stability between the source and the load, ensuring no oscillations or control 'hunting' occur during rapid power transitions or under normal load conditions.	
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## Step 2: Materials, Safety, and Compliance Disclosure

Partner must complete disclosure tables for:

### 2.1 Battery and PCS Materials and Safety

- Cell chemistry, enclosure type, fire detection/suppression approach.
- Cooling method (air/liquid), coolant type (if applicable).
- Dielectrics/insulation class for major components.
- Hazardous materials declaration (electrolyte class, refrigerants).

### 2.2 Standards and Regulatory Compliance Evidence

Provide certificates or reports for:

- UL 9540 / UL 9540A (or equivalent) status.
- NFPA 855 alignment statement.
- IEEE 2800 functional alignment statement (even if not certified).
- CE/UKCA (where applicable).
- RoHS/REACH.
- EMC compliance evidence relevant to PCS.

# Step 3: Core Requirements Availability

A subset of requirements are designated Core Requirements representing minimum essential capabilities to pass qualification. Partners must complete the "Core Requirements Checklist" provided in Appendix B.

Table 2. Core Requirements (Minimum)

No.	Core Requirement	Requirement ID	Minimum Requirement
1	Autonomous Island Operation Capability	CTRL-CORE-01	PCS shall stably transition to and sustain island mode operation. Loss of external voltage reference shall not cause voltage and frequency regulation to exceed specified performance limits. Voltage source behavior under current limit. Defined virtual impedance or equivalent mechanism.
2	AI Buffering Dynamic Response	PERF-CORE-01	Demonstrate active ramp-rate smoothing to buffer the source from sudden AI load swings. The system must maintain constant stability between the source and the load, ensuring no oscillations or control hunting occur during rapid power transitions or under normal load conditions.
3	Current Limit Behavior	PERF-CORE-02	Current limiting shall be predictable: no unstable oscillation, no uncontrolled voltage collapse in modeled grid conditions.
4	LVRT/HVRT	GRID-CORE-01	Support IEEE 2800 ride-through behavior as baseline; utility curves may supersede.
5	Reactive Power Support	GRID-CORE-02	Provide voltage support via Q within PCS current limits; document Q priority rules.
6	Seamless Grid/Island Transition	MODE-CORE-01	Demonstrate controlled transitions without loss of synchronism or unstable control mode hunting. Transition performance shall be quantified using voltage deviation per ANSI C84.1 and dynamic voltage/frequency ride-through per IEEE 2800.

7	Black Start	MODE-CORE-02	Demonstrate black-start energization of a dead bus and stable V/f regulation.
8	Telemetry and Controls	TELE-CORE-01	Real-time reporting of V, I, P, Q, f, SOC, alarms, and limit states. Must support 3 concurrent Modbus TCP connections with all points polled at 1 second frequency. SOC values must be included in all telemetry reporting.
9	Control Transparency Artifacts	MODEL-CORE-01	Provide EMT model + validation against impedance of admittance scan dq impedance vs frequency + Nyquist/passivity artifacts. Comply with NERC Reliability Guidelines.
10	DR Dispatch Capability	OPS-CORE-01	Follow dispatch setpoints with defined response time, ramp limits, and SOC reserve logic.

## Step 4: Qualification Tests

This section defines test procedures and pass/fail criteria. All tests are performed at the BESS AC terminals unless explicitly stated as model-only.

[Insert BESS Qualification Boundary diagram]

## Instrumentation Requirements

Minimum measurement accuracy (applies to all tests):

Parameter	Minimum Accuracy	Sampling Rate
Voltage	±0.2% of reading	≥ 5 kHz (EMT) / ≥ 10 Hz (operational)
Current	+/- 0.2%	≥ 5 kHz (EMT) / ≥ 10 Hz (operational)
Power (P/Q)	+/- 0.5%	≥ 10 Hz
Frequency	±0.01 Hz	≥ 10 Hz
Time Sync	±1 ms between channels	N/A

P/Q Dynamic (ramp, oscillations and transients)	+/- 0.1% of rated P at test frequency	>= 120 hz
Bandwidth	0.1-59.9 Hz	

All events must include pre-trigger ( $\geq 5$  s) and post-trigger ( $\geq 20$  s) unless otherwise specified.

## Test 1: Telemetry Verification and Data Integrity

Objective: Verify PCS telemetry accuracy, timestamping, and completeness.

Test Steps:

1. Operate PCS at 10%, 50%, 75% and 100% rated MW in grid-connected mode.
2. Record internal telemetry and compare to external 0.5S (IEC 62053-22) or better revenue-grade meters.
3. Verify by demonstration reporting of: V, I, P, Q, f, SOC, PCS temperature, current limit flags, and mode state.
4. Event logging shall be 1 ms precision.
5. Logs shall be held for 7 days minimum.
6. Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- P and Q error  $\leq \pm 0.5\%$  or better of reading across points.
- Time alignment error  $\leq 5$  ms.
- No missing channels, no flatlined sensors.

## Test 2: Grid-Adaptive Voltage and Frequency Regulation (Islanded)

Objective: Demonstrate stable operation with no external grid reference.

Setup: Isolated test bus with configurable resistive/inductance/capacitance (RLC) load bank.

Test Steps:

1. Black start onto dead bus (if Test 10 not yet done, run at reduced voltage).
2. Hold voltage and frequency within the system's defined stability limits at a steady load.
3. Apply load steps: +10%, +20%, -20% of PCS rated MW.
4. Record V, I, P, Q, f, and control mode state throughout the test.

5. Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- Stable V/f with no sustained oscillation.
- Voltage and frequency return to their steady-state range in a timely, well-damped manner, with no evidence of control hunting or marginal stability.
- No protective trip.

## Test 3: Current Limit Characterization (P-first, Q-first, and Mixed Priority)

Objective: Demonstrate stable, predictable, and transparent PCS behavior when operating at or beyond current limits under all priority configurations.

Test Steps:

1. Force the PCS into current limit using:
  - (a) Reduced-voltage condition on the test bus, or
  - (b) Commanded P and/or Q beyond the declared capability envelope.
2. Repeat for each priority configuration:
  - Active power (P) priority
  - Reactive power (Q) priority
  - Partner default or "grid-support" mode
3. Record P, Q, V, I, current-limit flags, and control-mode state variables.
4. Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- PCS remains stable and controllable while in current limit.
- PCS explicitly reports entry into and exit from current limit via telemetry.
- Control priority and available headroom are observable and consistent with documented behavior.

Disqualification Criteria:

- Limit-cycle oscillation: Under steady-state operating conditions, no sustained oscillations shall be present, and PCS performance shall remain within all applicable generator and grid interconnection requirements.
- Control-mode hunting: More than one control-mode transition (e.g., P→Q→P, GFM→GFL, or equivalent) during a single current-limit event constitutes test failure.
- Voltage recovery behavior: Upon release from current limit, terminal voltage shall recover monotonically to its regulated setpoint. Any overshoot, undershoot, or oscillatory recovery exceeding  $\pm 5\%$  of nominal voltage constitutes test failure.

Deliverables:

- P-Q capability map with clearly defined current-limit envelope.
- Annotated time-series plots showing: entry into current limit, behavior while limited, exit from current limit and voltage recovery.
- Description of current-limit implementation and priority logic.
- Demonstrate through EMT analysis.

## Test 4: AI Buffering Proxy Test (Fast Ramp Tracking)

Objective: Demonstrate the BESS can buffer AI-induced power ramps at the required rate without inducing control instability.

Test Steps:

1. Operate PCS in grid-connected mode at both weak-grid ( $SCR \leq 3$ ) and strong-grid ( $SCR \geq 20$ ) configurations
2. Apply a time-varying active power command profile that is representative of realistic AI workload ramps, including both short bursts and longer ramp intervals, and reaching ramp rates up to the vendor's declared AI-buffering capability. Partner must state the assumed IT load used for the test and demonstrate correct scaling of results.
3. Record P, Q, V, I, and current-limit and control-mode state flags.
4. Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- Tracking accuracy: Steady-state ramp tracking error  $\leq 2\%$  of commanded ramp magnitude.
- Current limit: No entry into current limit during execution of required buffering profile.
- Stability: No sustained oscillatory behavior induced by control interaction.

Disqualification Criteria:

- Sustained oscillation: Any clearly observable, sustained oscillatory behavior in measured P, Q, V, I, or frequency that indicates marginal or unstable control response during the ramp profile constitutes test failure, regardless of steady-state tracking accuracy.
- Current-limit interaction: Repeated or sustained entry into current limit, as indicated by PCS telemetry or limit-state flags, during execution of the required buffering profile constitutes test failure, unless explicitly declared as outside the partner's stated capability envelope.
- Ringing tolerance: Short-duration transient ringing ( $< 1$  s) is acceptable only if it is monotonically decaying, does not re-enter current limit, and does not induce control-mode transitions.

Note: This test does not, by itself, prove site POI compliance. It verifies that the PCS can execute the required buffering action when properly integrated.

## Test 5: AI Buffering EMT Validation (Model-Based, Required)

Objective: Validate PCS stability and control robustness under extreme weak-grid conditions representative of faulted, partially islanded, or switching-dominated AI campus scenarios.

Partner Provides:

- EMT model of PCS + controls (compiled or encrypted acceptable, but must run).
- dq impedance curves vs frequency.
- Nyquist or passivity evidence.

Required EMT Case:

- SCR: 2.0.
- Grid impedance: Sweep from X/R ratio = 2 to 10, representative of inverter-dominated grids.
- Topology: Grid-connected with upstream source modeled as weak voltage source.
- Load: Constant Power Load representative of IT/compute with clearly defined ramp characteristics shall be used.

Disturbances to Apply:

- AI buffering proxy ramps.
- At least one grid disturbance event (voltage dip, impedance step, or partial islanding).
- Entry into and recovery from PCS current limit.

Test Steps:

1. Configure the EMT model with the required case parameters above.
2. Apply each disturbance scenario sequentially, recording all state variables.
3. Provide all model outputs and analysis necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- POI ramp compliance for the defined workload profile.
- No unstable oscillation modes across operating range.
- System remains stable with no loss of synchronism.
- No sustained oscillatory modes.
- No uncontrolled voltage collapse at the BESS terminals.
- PCS transitions into and out of current limit in a controlled and documented manner.

Failure Criteria:

- Any unstable oscillation persisting > 1 second.
- Voltage collapse or failure to recover to regulated operating point.
- Control mode hunting or undefined control state transitions.
- Model instability that prevents completion of the test scenario.

This stress case may be performed model-only. Failure in this case constitutes non-qualification, regardless of performance at higher SCR values. This test is intended to expose control fragility under realistic worst-case grid conditions expected in large AI campus deployments.

## Test 6: Demand Response Dispatch Performance

Objective: Verify DR execution without breaking buffering and ride-through reserves.

Test Steps:

1. Demonstrate dispatch steps at: 10%, 25%, 50%, and 100% of DR committed MW.
2. Demonstrate ramp-limited dispatch (partner must implement ramp limits).
3. Demonstrate SOC reserve policy: hold back prescribed SOC capacity reserved for LVRT/buffering.
4. Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- Commanded MW achieved within specified response time (default: 2 s for fast DR, 60 s for slow DR).
- No violation of SOC reserve rules.
- Clear state machine behavior when DR conflicts with LVRT.

Deliverable: DR state machine diagram and priority rules.

## Test 7: LVRT/HVRT Functional Ride-Through (Hardware or HIL)

Objective: Prove ride-through behavior aligned to IEEE 2800 baseline.

Test Steps:

1. Apply voltage sag and swell profiles at AC terminals (grid simulator or HIL) at both weak-grid ( $SCR \leq 3$ ) and strong-grid ( $SCR \geq 20$ ) configurations: multiple depth-duration points per IEEE 2800 or utility categories.
2. Observe whether PCS stays connected and how it prioritizes Q support.
3. Record V, I, P, Q, f, and protection relay states throughout each ride-through event.
4. Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- No trip within IEEE envelope or applicable utility/ISO envelope, whichever governs
- Correct trip outside envelope.
- Q injection behavior documented and consistent.

## Test 8: Seamless Grid/Island Transition

Objective: Validate transition logic and stability.

Test Steps:

1. Start grid-connected in buffering mode.
2. Execute intentional islanding event (open upstream breaker) while load present.
3. Maintain V/f and continue supplying load.
4. Resynchronize and reconnect to grid with controlled closing logic.
5. Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- No unstable mode hunting.
- No uncontrolled frequency drift.
- Reclose without excessive inrush or protective trips.
- Event logs show proper sequencing.

## Test 9: Islanded Operation with Generator Following (Model-Based)

Objective: Validate interaction with turbines or gensets.

Test Steps:

1. EMT model with GFM BESS as voltage master.
2. Generator modeled as droop-following source with realistic governor time constants.
3. Apply AI load proxy disturbance and show: (a) BESS absorbs fast dynamics, (b) Generator picks up slower energy component.
4. Include N-1 generation event.
5. Provide all model outputs and analysis necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- No sustained oscillation.
- SOC drift controlled (see Test 11).
- Frequency and voltage remain within declared bounds.

## Test 10: Black Start

Objective: Demonstrate ability to energize a dead bus and establish stable V/f.

Test Steps:

1. PCS starts from de-energized condition.
2. Energize test bus to nominal voltage.
3. Pick up load in steps: 10%, 25%, 50% rated.
4. If using auxiliary supply, document requirements.
5. Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- Stable energization.
- No nuisance trips.
- V/f regulation within declared bounds.

## Test 11: SOC Drift and Energy Management Under Combined Missions

Objective: Demonstrate that the BESS can simultaneously support AI buffering, demand response, and LVRT reserve obligations over time without uncontrolled state-of-charge (SOC) drift.

Test duration: Minimum 24-hour continuous simulation or accelerated profile test.

Test Steps:

1. Run a 24-hour simulation or accelerated profile test with: AI buffering proxy ramps applied intermittently throughout the test window, demand response dispatch events of varying magnitude and duration, at least one LVRT or equivalent grid-disturbance event, and declared SOC operating window and reserve thresholds enforced.
2. Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria:

- Net SOC drift:  $\leq \pm 5\%$  of usable SOC capacity, excluding declared DR events.
- SOC bounds: Remain within partner-declared operating window at all times.
- Energy prioritization: Explicit de-prioritization when approaching reserve thresholds.

Disqualification Criteria:

- Unbounded SOC drift: Exceeding  $\pm 5\%$  without declared external energy imbalance.
- Undefined reserve behavior: Loss of capability without explicit state transition.

- Implicit behavior: SOC management relying on undocumented heuristics.

Required Deliverables:

- Time-series plots of SOC, P, Q, service state, and reserve flags.
- Energy balance summary table (in/out, losses, DR energy, net drift).
- State machine diagram showing: normal operation, reserve-threatened operation, de-rating or service shedding behavior.
- Event log with timestamped state transitions and priority changes.

Oversizing battery capacity alone does not satisfy this requirement. SOC stability must be achieved through control logic and energy management, not nameplate capacity.

## Test 12: Control Transparency Package Review

Objective: Provide the analysis artifacts needed for integration.

Required Deliverables:

- EMT model package with instructions.
- dq or sequence (full matrix) impedance vs frequency (magnitude and phase) in key operating points at least at +0.9 p.u and - 0.9 p.u. Active power.
- Nyquist plot or passivity assessment demonstrating stability margin for extremely weak (SCR = 2, X/R = 10) and strong grid conditions (SCR = 20, X/R = 10).
- Controller description: loops, bandwidths, current limit behavior.
- Parameter list: droop coefficients, virtual impedance, inertia, PLL state (if any).

Pass Criteria:

- Package is complete, runnable, and consistent with measured behavior.
- No "black box with no stability evidence" accepted.
- Have snapshot feature to start simulations from a specific snapshot
- Model runs with generally accepted Fortran compilers released after 2018.

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# Business and Supply Chain Readiness

In addition to technical qualification, partners must demonstrate credible readiness to support AI-scale deployment timelines. This includes proven manufacturing throughput, realistic ramp capability, and supply chain resilience aligned with multi-hundred-MW to GW-scale deployments.

## 4.1 Demonstrated Manufacturing Throughput

Partners must disclose actual, historical production capability, not theoretical capacity.

Required Disclosures:

- Annual PCS throughput delivered in the most recent 12-month period (MW/year).
- Largest single PCS or BESS deployment delivered to date (MW and delivery timeframe).
- Current factory locations supporting PCS production and final integration.
- Current average and worst-case lead times for PCS delivery.

Evidence Required:

- Shipment records or customer references.
- Factory acceptance test (FAT) throughput data.
- Identification of binding constraints (labor, test infrastructure, power electronics, controls).

## 4.2 Scale Ramp Credibility (10x Within 24 Months)

Partners must present a credible, executable plan to scale PCS manufacturing throughput by an order of magnitude (10x) within 24 months.

Required Elements:

- Baseline throughput (MW/year) and target throughput (MW/year).
- Time-phased ramp plan with quarterly milestones.
- Critical path items: power semiconductor supply, control hardware, test infrastructure, labor.
- Capital investments required (facilities, tooling, test equipment).
- Dependencies on single-source or constrained sub-suppliers.

## 4.3 Supply Chain Resilience and Risk Disclosure

Required Disclosures:

- Single-source components and mitigation plans.
- Geographic concentration risks (manufacturing, sub-tiers).
- Long-lead components and committed capacity.
- Inventory buffering strategy for critical components.
- Exposure to export controls, trade restrictions, or geopolitical risk.

## 4.4 Failure Mode Acknowledgment

Partners must explicitly identify scenarios in which scale targets cannot be met.

- Conditions under which throughput ramp would be delayed or capped.
- Contingency plans and alternative sourcing strategies.
- Clear articulation of commitments under accelerated demand scenarios.

## 4.5 Industrial Standards and Regulatory Certificates

Partners must provide a list of industrial standards the system is designed to comply with (e.g., IEEE, IEC, GB), as well as test certificates (e.g., UL, CSA, CE, CCC) granted by countries or economic areas for installation and operation.

Lack of demonstrated historical throughput or absence of a credible scale-up plan constitutes business non-qualification, regardless of technical performance. This section is intended to surface manufacturing reality early, not after technical qualification.

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# Quality and Reliability

This section defines the minimum quality system evidence and reliability substantiation required for BESS qualification. The intent is to prevent "passes on paper" where functional tests succeed but field reliability is unacceptable.

## 5.1 Quality Management System and Traceability

Required Submissions:

- QMS certification: ISO 9001 certificate (or equivalent), including scope and certified sites.
- Change control process: Documented ECN/ECO process with revision control.
- Supplier quality: Supplier qualification process, incoming inspection, SCAR workflow.
- Traceability: Lot traceability for battery cells, power semiconductors, capacitors, magnetics, control boards.
- Serialization: Unique serial numbers at rack, PCS, and critical subassembly level.
- Nonconformance system: NCR process, RCA expectations, and closure criteria.
- CAPA: Metrics and example packages from the last 12 months.

## 5.2 Reliability Targets and Definitions

Minimum Required Declarations:

- Availability target for the qualified configuration.
- MTBF / MTTF definitions and calculation method.
- Failure rate assumptions and confidence bounds.
- AFR for major replaceable units (PCS power stage, controller, cooling system, BMS, contactors).
- Mission profile including ambient range, load profile, switching frequency, current-limit time fraction, SOC window.

If the partner cannot defend reliability numbers under an AI buffering duty cycle, the system fails qualification regardless of lab functional results.

## 5.3 Reliability Model and Evidence Requirements

- Reliability block diagram (RBD) showing system topology and redundancy.
- FMEA/DFMEA and PFMEA with top 20 risk items and mitigations.
- Parts stress and thermal analysis for the PCS.
- Reliability prediction method and justification.
- Field reliability evidence (if product is deployed).

## 5.4 Environmental and Durability Qualification

- Thermal performance and derating curves.
- Thermal cycling test results.
- Vibration and shock testing (ISTA or IEC 60068 equivalent).
- Ingress protection (IP/NEMA rating evidence).
- Corrosion / contamination robustness.
- Acoustic and mechanical resonance risks.

## 5.5 Power Electronics Reliability and Protection Robustness

- Protection coordination philosophy inside the PCS.
- Short-circuit and fault withstand capability.
- Grid disturbance robustness.
- Harmonic and ripple limits.

## 5.6 Battery System Reliability and Safety Monitoring

- Cell and module qualification basis.
- BMS robustness and fault detection coverage.
- Thermal management reliability.
- Degradation model and capacity fade predictions, including degradation rates based on shallow discharges at a variety of SOC levels.
- Maintenance intervals and remote diagnostics capability.

## 5.7 Factory Acceptance, Production Testing, and Burn-In

- Factory Acceptance Test (FAT) procedure.
- Production test coverage (every unit vs sampling).
- Burn-in or screening for infant mortality.
- Calibration and metrology schedule.

## 5.8 Serviceability, Spares, and Mean Time to Repair

- MTTR assumptions and basis.
- Spare parts list with recommended on-site spares.
- Replaceable unit strategy and hot-swap capability.
- 24/7 remote support model and escalation process.
- Event logging requirements and export format.

## 5.9 Reporting Format and Acceptance Criteria

Partners must submit a single Quality and Reliability Package containing:

- QMS certificates and site scope.
- Reliability model (RBD + assumptions) and results.

- DFMEA/PFMEA top risks and mitigations.
- Environmental qualification reports.
- FAT and production test summaries.
- Field reliability data with failure mode breakdown.
- Maintenance plan, MTTR basis, and spares strategy.

Automatic Fail Conditions:

- Missing QMS/traceability evidence.
- Reliability predictions not tied to a declared mission profile.
- Failure to provide DFMEA/PFMEA and top-risk mitigations.
- Field data contradicts claims without explanation and corrective plan.

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## Appendices

### Appendix A: Data Submission Requirements

Every test must include:

- Raw time-series (CSV).
- Summary plots (PDF).
- Test configuration (single-line of test setup, controller settings, SOC).
- Pass/fail statement tied to criteria.
- Known issues and deviations list.

### Appendix B: Core Requirements Checklist

Partner must fill out a one-page checklist mapping: Core Requirement → Test IDs → Evidence references.

# Appendix C: Partner Model Package Requirements

Minimum:

- EMT model (PSCAD/EMTDC, RTDS, or equivalent), including control blocks.
- dq impedance plots at: 10%, 50%, 100% P; High and low Q; Multiple SCR values.
- Nyquist/passivity artifact and interpretation.
- Version-controlled parameter export.

Models that cannot reproduce hardware behavior within stated tolerances are invalid.

# Appendix D: Industrial Standards and Regulatory Certificates

Partners must provide a list of industrial standards the system is designed to comply with, as well as test certificates granted by countries or economic areas. Key standards include:

- IEEE 1547-2018, IEEE 2800.
- UL 9540 / UL 9540A.
- NFPA 855.
- CE/UKCA.
- RoHS/REACH.
- IEC 60068.
- ISO 9001.
- NERC Reliability Guidelines.
- NERC CIP (Critical Infrastructure Protection).
- IEC 62443 (Industrial Automation and Control Systems Security).
- NIST Cybersecurity Framework (CSF).

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# Appendix E: DCE BESS Equipment Qualification Process

NVIDIA defines the bar. Independent testing labs verify. OEMs prove compliance directly to their customer. Marketplace listing is recognition of a process completed — not the gate that allows it.

## Roles with Qualification vs. Listing

**Nvidia:** Authors the criteria. Hosts the marketplace. Reviews the lab report at the end of the cycle. Publishes PRD & test procedures, qualifies third-party labs, reviews final compliance package, lists qualified product (best effort).

**BESS OEM:** Designs and builds the BESS. Owns compliance — responds line by line and engages the lab. Responds to PRD (C / D / E), provides EMT model & disclosures, contracts an approved test lab, presents results to customer.

**Test lab:** Can be inhouse or Independent of the OEM, with Nvidia approvals. Executes the twelve qualification tests and issues the compliance report. Bench, HIL, factory or field test, EMT model validation, Raw data + plots per Appendix A, Per-test pass / fail with evidence

**Customer:** Reviews the lab report against site needs. Issues the site acceptance that unlocks deployment. Reviews compliance evidence, Validates site-level integration, Commissions in the field, Issues site acceptance

The following steps outline the process to submit completed test reports to Nvidia for listing into its Marketplace website.

## Step 1: Login to NVOnline

Navigate to the NVOnline portal. From the top navigation bar, select the appropriate Site for your company. Use the Content Library to access reference documents such as platform design guides and related specifications.

### 1. Login NVOnline

The screenshot shows the NVIDIA NVOnline Content Library interface. At the top, there is a navigation bar with the NVIDIA logo and 'NVONLINE' text. To the right, there are dropdown menus for 'Site' (set to 'MGX\_Foxconn') and 'Tinker Tsai'. Below the navigation bar, there is a 'CONTENT LIBRARY' header. A search bar is present with the placeholder text 'Enter keywords here or apply filters below' and a 'SEARCH' button. On the left side, there are filter sections for 'Product Line' (with options for HGX and MGX), 'Content Class' (with an option for Platform), 'Product Family' (with options for GB200 NVL, HGX B100, and HGX B200), and 'HW Platform/SW Release'. The main content area displays a list of documents with their titles, posting dates, and 'Download' links. The documents listed are: 'MGX GB200 Bianca Cold Plate CAD and Thermal Test S...', 'GB200 MGX Rack Mounting Kit for CC and Manifold, L...', 'NVIDIA Blackwell HGX 8-GPU Platform Design Guide', and 'MGX GB200 FullRack 44RU Manifold CAD'. At the bottom of the page, there is a footer with links for 'Privacy Policy', 'Manage My Privacy', 'Do Not Sell or Share My Data', 'Accessibility', 'Corporate Policies', 'Product Security', and 'Terms of Use', along with the copyright notice 'Copyright © 2024 NVIDIA Corporation.'

## Step 2: Navigate to Report a Bug

From the NVOnline homepage, click on the "Bug" menu in the top navigation bar and select "Report a Bug" from the dropdown menu.

## 2. Find Bug -> Report a Bug

The screenshot shows the NVIDIA NVONLINE portal interface. At the top, the NVIDIA logo and 'NVONLINE' text are visible. The user is logged in as 'Tinker Tsai' at the 'MGX\_Foxconn' site. The navigation menu includes 'HOME', 'BUG', and 'HELP'. The 'BUG' menu is highlighted with a red circle, and a dropdown menu is open, showing 'Report a Bug' and 'View Bug Status'. Below the navigation, there is a search bar with the text 'Jump to bug id.' and a 'Go' button. The main content area displays a list of bugs with filters on the left and pagination controls at the top. The bugs listed include 'MGX GB200 Bianca Cold Plate CAD and Thermal Test S...', 'GB200 MGX Rack Mounting Kit for CC and Manifold, L...', 'NVIDIA Blackwell HGX 8-GPU Platform Design Guide', and 'MGX GB200 FullRack 44RU Manifold CAD'.

## Step 3: Fill in the Bug Report Form

Complete the "Report a Bug" form.

### Common Form Fields

- Problem Type: Select "Qualification Review" from the dropdown.
- Severity: Low.
- Priority: 3 - Low.
- Divisions: Select your company site from the dropdown.
- Issue Type: Select "Qualification-Review-Issue".
- Product Segment: Select "Other".
- Focus Area: Select "DC Infrastructure" and then "BESS" from the subcategory dropdown.

### Synopsis Format by Use Case

The Synopsis field (200 characters maximum) must follow one of these formats:

- Qualification Review: Facilities Level - <Supplier Company Name> DC Infrastructure BESS Review

## Step 4: Enter BESS-Specific Description (Qualification Review)

For Qualification Review submissions, enter the following information in the Description field. Items marked with <attachment> must be uploaded as file attachments:

1. Subject: Facilities Level - <Supplier Company Name> DC Infrastructure BESS Review
2. MPN: <Supplier part number>
3. Revision: <version>
4. SPEC: Supplier SPEC <attachment>
5. 3D CAD: Supplier CAD <attachment>
6. 2D Drawing: Supplier 2D <attachment>
7. Self Validation Report: Supplier performance validation report per BESS Self-Validation Guidelines <attachment>

## Step 5: Add Members, Upload Attachments, and Submit

Before submitting the bug, complete the following:

1. Add Members: In the Cc Details section, add all relevant NVIDIA and partner team members who should be notified of this submission.
2. Upload Attachments: In the Attachments section, drag and drop or browse to upload all design files referenced in the description (SPEC, 3D CAD, 2D Drawing, Self Validation Report).
3. Submit: Once all details are filled in and attachments are uploaded, click the "Submit Bug" button. You may also use "Save as draft" to save your progress before submitting.





## Step 6: View Bug Status and Add Comments

After submitting, you can track your submission and provide additional information:

1. View Bug Status: Navigate to Bug > "View Bug Status" in the top menu. Search by Bug ID, synopsis, or other criteria. Click on the Bug ID to view full details.
2. Add Comments: From the bug detail page, scroll to the Comment Log section and click "Add Comment" to upload additional attachments or provide updates.

All information submitted is confidential and only viewable between the submitting partner and NVIDIA.

## NVBug Notifications

Users will receive system notifications (via email) whenever there is an update on their NVBug submission. These notifications include status changes, new comments, and resolution updates. This applies to both Qualification Review and RFI submissions.

## NVOnline Site Setup for Partners

Partners must have their NVOnline site properly configured to submit qualification bugs. The site must be set with "Customer Bug Forms Setup" enabled. The Qualification Review Bug Forms / Problem Types must be activated.

Ensure the "Active" checkbox is checked. Contact your NVIDIA partner representative if your site is not configured correctly.

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