



# cuDNN Best Practices

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# Chapter 1. Introduction



**ATTENTION:** These guidelines are applicable to 3D convolution and deconvolution functions starting in NVIDIA® CUDA® Deep Neural Network library™ (cuDNN) v7.6.3.

This document provides guidelines for setting the cuDNN library parameters to enhance the performance of 3D convolutions. Specifically, these guidelines are focused on settings such as filter sizes, padding and dilation settings. Additionally, an application-specific use-case, namely, medical imaging, is presented to demonstrate the performance enhancement of 3D convolutions with these recommended settings.

Specifically, these guidelines are applicable to the following functions and their associated data types:

- ▶ [cudnnConvolutionForward\(\)](#)
- ▶ [cudnnConvolutionBackwardData\(\)](#)
- ▶ [cudnnConvolutionBackwardFilter\(\)](#)

For more information, see the [cuDNN Developer Guide](#) and [cuDNN API](#).

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# Chapter 2. Best Practices For Medical Imaging

To optimize your performance in your model, ensure you meet the following general guidelines:

## **Layout**

The layout is in NCHW format.

## **Filter size**

The filter size is  $T \times 1 \times 1$ ,  $T \times 2 \times 2$ ,  $T \times 3 \times 3$ ,  $T \times 5 \times 5$ , where  $T$  is a positive integer. There are additional limits for the value of  $T$  in `wgrad` and `strided dgrad`.

## **Stride**

Arbitrary for forward and backward filter; `dgrad/deconv`:  $1 \times 1 \times 1$  or  $2 \times 2 \times 2$  with  $2 \times 2 \times 2$  filter.

## **Dilation**

The dilation is  $1 \times 1 \times 1$ .

## **Platform**

The platform is Volta, Turing, and Ampere with input/output channels divisible by 8.

## **Batch/image size**

cuDNN will fallback to non-Tensor Core kernel if it determines that the workspace required is larger than 256MB of GPU memory. The workspace required depends on many factors. For the Tensor Core kernels, the workspace size generally scales linearly with output tensor size. Therefore, this can be mitigated by using smaller image sizes or minibatch sizes.

## 2.1. Recommended Settings In cuDNN While Performing 3D Convolutions

The following tables show the specific improvements that were made in each release.

### 2.1.1. cuDNN 8.x.x

Recommended settings while performing 3D convolutions for cuDNN 8.x.x.

		8.0.0 - 8.0.1 Preview
Platform		<ul style="list-style-type: none"> <li>▶ NVIDIA Ampere GPU architecture</li> <li>▶ NVIDIA Turing GPU architecture</li> <li>▶ NVIDIA Volta GPU architecture</li> </ul>
Convolution (3D or 2D)		3D and 2D
Convolution or deconvolution ( <code>fprop</code> , <code>dgrad</code> , or <code>wgrad</code> )		<code>fprop</code> <code>dgrad</code> <code>wgrad</code>
Grouped convolution	Yes or No	Yes
	Group size	<code>C_per_group == K_per_group == {4, 8, 16, 32}</code>
Data layout format (NHW/NCHW) <sup>1</sup>		NDHWC
Input/output precision (FP16, FP32, or FP64)		FP16 and FP32 <sup>2</sup>
Accumulator (compute) precision (FP16, FP32, or FP64)		FP32
Filter (kernel) sizes		No limitation
Padding		No limitation
Image sizes		2GB limitation for a tensor
Number of channels	C	0 mod 8
	K	0 mod 8
Convolution mode		Cross-correlation and convolution
Strides		<code>dgrad</code> : 1x1x1 or 2x2x2
Dilation		No limitation

## 2.1.2. cuDNN 7.6.x

Recommended settings while performing 3D convolutions for cuDNN 7.6.x.

	7.6.5	7.6.4	7.6.2	7.6.1
Platform	Turing Volta	Volta		
Convolution (3D or 2D)	3D and 2D	3D		
Convolution or deconvolution ( <code>fprop</code> , <code>dgrad</code> , or <code>wgrad</code> )	<code>fprop</code> <code>dgrad</code> <code>wgrad</code>		<code>fprop</code> <code>dgrad</code>	<code>fprop</code> <code>dgrad</code> <code>wgrad</code>

<sup>1</sup> NHWC/NCHW corresponds to NDHWC/NCDHW in 3D convolution.

<sup>2</sup> With `CUDNN_TENSOROP_MATH_ALLOW_CONVERSION` pre-Ampere. Default TF32 math in Ampere.

		7.6.5	7.6.4	7.6.2	7.6.1
Grouped convolution	Yes or No	Yes		No	
	Group size	$C_{per\_group} ==$ $K_{per\_group} ==$ {4, 8, 16, 32}		NA	
Data layout format (NHWC/NCHW) <sup>3</sup>		NCDHW			NCDHW <sup>4</sup>
Input/output precision (FP16, FP32, or FP64)		FP16		FP16 or FP32	FP16 <sup>5</sup> or FP32 <sup>6</sup>
Accumulator (compute) precision (FP16, FP32, or FP64)		FP32		Better to be the same with input/output precision	FP32
Filter (kernel) sizes		2x2x2 T <sup>7</sup> x1x1 Tx2x2 Tx3x3 Tx5x5			1x1x1 2x2x2 3x3x3 5x5x5 Tx1x1 Tx2x2 Tx3x3 Tx5x5 Tx1x1 Tx2x2 Tx3x3 Tx5x5
Padding		No limitation			Filter // 2 <sup>8</sup>
Image sizes		256 MB WS limit		No limitation	256 MB WS limit
Number of channels	C	Arbitrary			0 mod 8
	K	Arbitrary			0 mod 8
Convolution mode		Cross-correlation for dgrad; otherwise, both modes		No limitation Cross-correlation	
Strides		1x1x1 and 2x2x2 strides for dgrad		2x2x2 Arbitrary stride	1x1x1

<sup>3</sup> NHWC/NCHW corresponds to NDHWC/NCDHW in 3D convolution.

<sup>4</sup> With NCHW <-> NHWC format transformation.

<sup>5</sup> FP16: CUDNN\_TENSOROP\_MATH

<sup>6</sup> FP32: CUDNN\_TENSOROP\_MATH\_ALLOW\_CONVERSION

<sup>7</sup> An arbitrary positive value.

<sup>8</sup> padding = filter // 2

	7.6.5	7.6.4	7.6.2	7.6.1
Dilation	1x1x1			

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# Chapter 3. Medical Imaging Performance

The following table shows the average speed-up of **unique cuDNN 3D convolution calls** for each network that satisfies the conditions in [Best Practices For Medical Imaging](#). The end-to-end training performance will depend on a number of factors, such as framework overhead, kernel run time, and model architecture type.

Model	Batchsize	Avg. Speed-up of unique cuDNN 3D convolution API calls (7.6.3 vs. 7.5.1)
V-Net (3D-Image segmentation)	2	4.4x
	4	4.4x
	8	4x
	16	4x
	32	4x
	64	3.4x
	128	3x
3D-UNet (3D-Image Segmentation)	2	4.4x
	4	4.1x
	8	4.4x
	16	4.3x
	32	4x
	64	4x
	128	4.2x



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## Chapter 4. Medical Imaging Limitations

Your application will be functional but slow if the model has:

- ▶ Channel counts lower than 32 (gets worse the lower it is)
- ▶ Data gradients for convolutions with stride

If the above is in the network, use `cuDNNFind` to get the best option.

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