MCP7Y70-Hxxx 400Gb/s Twin-port 2x200G OSFP to 4x100G QSFP56 DAC Splitter Product Specifications

Exported on Dec/03/2023 12:44 PM

Table of Contents

Introduction

NVIDIA® MCP7Y70 is a passive Direct Attach Copper (DAC) cable with an OSFP-based twin-port 2x 200Gb/s connector to four 200Gb/s QSFP56s, and is a high-speed 100Gb/s splitter cable for InfiniBand and Ethernet networking. The DAC firmware supports both InfiniBand and Ethernet and is automatically enabled depending on the protocol of the switch attached to.

The 8-channel twin-port OSFP end uses a finned top form-factor for use in Quantum-2 and Spectrum-4 switch cages. The four 100G ends support 2-channels of 50G-PAM4 (100GbE/HDR100) and use a flat top QSFP56 for use in ConnectX-6/7 adapters and BlueField-2/3 DPUs using riding heat sinks on the connector cage.

DAC cables are the lowest-cost, lowest-latency, near zero power consuming, high-speed links available due to their simplicity of design and minimal components. The “passive” term refers to the copper cable containing no electronics in the data path. Each end includes an EEPROM which provides product identification and characteristics to the host system. Every cable length is tuned to reduce internal signal noise and back reflections. Thin 30AWG is used for 1 and 1.5-meter lengths and thicker 26AWG for 2-meters.

Main use is linking Quantum-2 NDR InfiniBand and Spectrum-4 Ethernet switches to HDR100/100GbE switches, ConnectX-6/7 adapters, and/or BlueField-2/3 DPUs up to 2-meters.

NVIDIA’s cable solutions provide power-efficient connectivity enabling higher port bandwidth, density and configurability at a low cost and reduced power requirement in the data centers. Rigorous cable production testing ensures best out-of-the-box installation experience, performance, and durability.

Images are for illustration purposes only. Product labels, colors, and lengths may vary.

Key Features

- 400Gb/s to four 100Gb/s data rates
- Based on 2-channel 50G-PAM4 modulation
- 1, 1.5, and 2-meter lengths
- OSFP and QSFP112 ends each consume 0.1 Watts
- OSFP head end is CMIS based
- QSFP112 ends are SFF-8636 based
- Operating case temperature 0-70°C
- Single 3.3V supply voltage
- Hot pluggable
- RoHS compliant
- LSZH (Low Smoke Zero Halogen) jacket
- LF (Lead Free) HF (Halogen Free) PCB
- OSFP and SFF-8665 compliant
- SFF-8636 compliant I^2C management interface (QSFP ends)
- CMIS compliant I^2C management interface (OSFP end)

Applications

- 2x200G 2xHDR InfiniBand Quantum-2 or Spectrum-4 Ethernet switch-to-four 100Gb/s switches, QSFP28/56/112

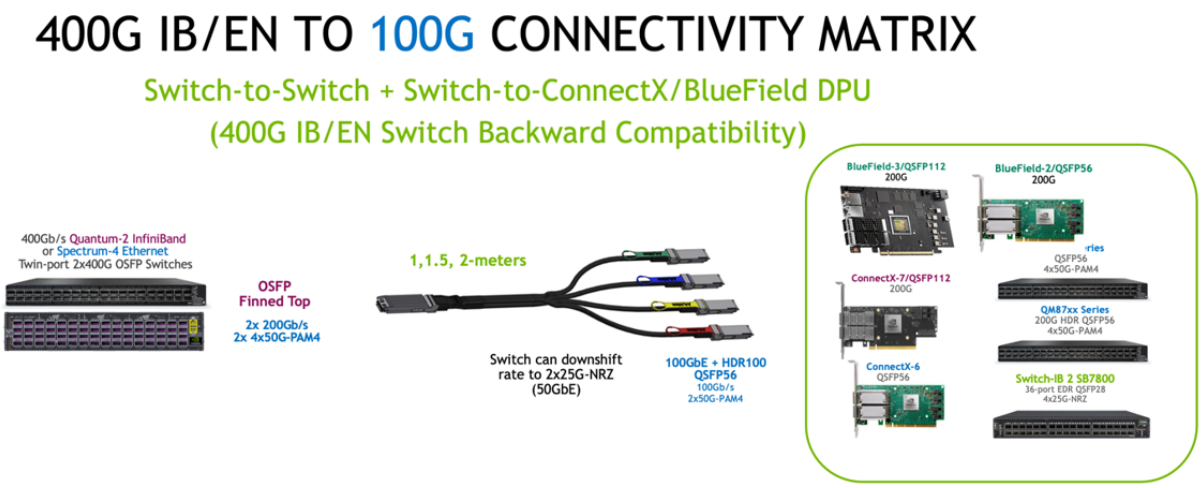
ConnectX-5/6/7,
and/or
BlueField-2/3 DPUs

Overview

Use Cases

The MCP7Y70 is used to connect Quantum-2 NDR InfiniBand and 400GbE Ethernet switches to Quantum based switches, ConnectX-6/QSFP56 adapters, and/or BlueField-2 DPUs spanning up to 2-meters.

- Both a ConnectX-6 and BlueField-2 DPU can be linked at the same time.
- 2x200G DAC can downshift the HDR100 InfiniBand 2x50G-PM4 rate to 2x25G-NRZ or 50GbE.



Pin Descriptions

The device is is compliant with the Specification for OSFP (Octal Small Form Factor Pluggable) Modules for the head end (www.osfpmsa.org) and the SFF-8636 specification for the tails (www.snia.org/technology-communities/sff/specifications).

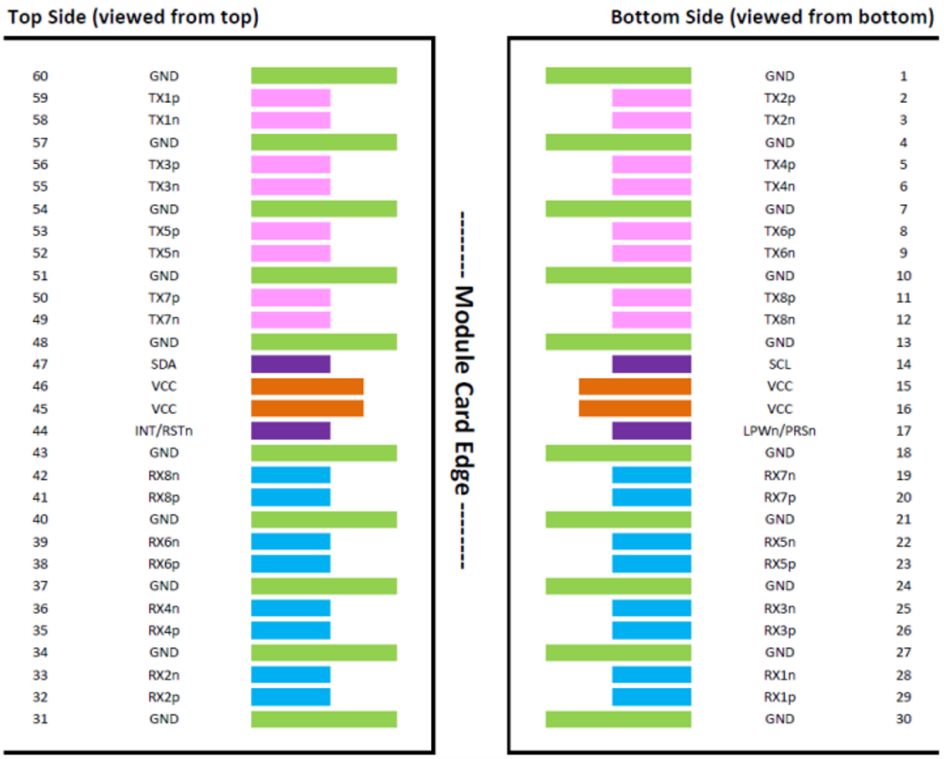
The pin assignment for the interface is shown below.

OSFP Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	31	GND	Ground
2	Tx2p	Transmitter Non-Inverted Data Input	32	Rx2p	Receiver Non-Inverted Data Output
3	Tx2n	Transmitter Inverted Data Input	33	Rx2n	Receiver Inverted Data Output
4	GND	Ground	34	GND	Grounds
5	Tx4p	Transmitter Non-Inverted Data Input	35	Rx4p	Receiver Non-Inverted Data Output
6	Tx4n	Transmitter Inverted Data Input	36	Rx4n	Receiver Inverted Data Output
7	GND	Ground	37	GND	Ground
8	Tx6p	Transmitter Non-Inverted Data Input	38	Rx6p	Receiver Non-Inverted Data Output
9	Tx6n	Transmitter Inverted Data Input	39	Rx6n	Receiver Inverted Data Output
10	GND	Ground	40	GND	Ground
11	Tx8p	Transmitter Non-Inverted Data Input	41	Rx8p	Receiver Non-Inverted Data Output
12	Tx8n	Transmitter Inverted Data Input	42	Rx8n	Receiver Inverted Data Output
13	GND	Ground	43	GND	Ground
14	SCL	2-wire serial interface clock	44	INT / RSTn	Module Interrupt / Module Reset
15	VCC	+3.3V Power	45	VCC	+3.3V Power
16	VCC	+3.3V Power	46	VCC	+3.3V Power
17	LPWn / PRSn	Low-Power Mode / Module Present	47	SDA	2-wire Serial interface data
18	GND	Ground	48	GND	Ground
19	Rx7n	Receiver Inverted Data Output	49	Tx7n	Transmitter Inverted Data Input
20	Rx7p	Receiver Non-Inverted Data Output	50	Tx7p	Transmitter Non-Inverted Data Input
21	GND	Ground	51	GND	Ground
22	Rx5n	Receiver Inverted Data Output	52	Tx5n	Transmitter Inverted Data Input

Pin	Symbol	Description	Pin	Symbol	Description
23	Rx5p	Receiver Non-Inverted Data Output	53	Tx5p	Transmitter Non-Inverted Data Input
24	GND	Ground	54	GND	Ground
25	Rx3n	Receiver Inverted Data Output	55	Tx3n	Transmitter Inverted Data Input
26	Rx3p	Receiver Non-Inverted Data Output	56	Tx3p	Transmitter Non-Inverted Data Input
27	GND	Ground	57	GND	Ground
28	Rx1n	Receiver Inverted Data Output	58	Tx1n	Transmitter Inverted Data Input
29	Rx1p	Receiver Non-Inverted Data Output	59	Tx1p	Transmitter Non-Inverted Data Input
30	GND	Ground	60	GND	Ground

OSFP Module Pad Layout

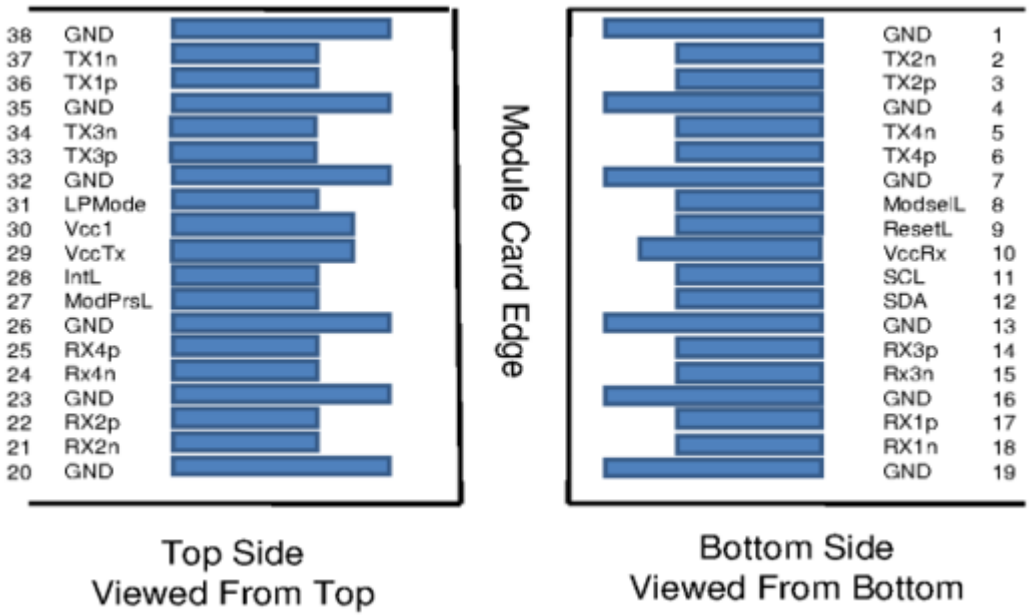


QSFP56 Pin Description

The MCP7Y60 pin assignment is SFF-8679 compliant for the two 200G ‘tails’ with QSFP56 form factor:

Pin	Symbol	Description	Pin	Symbol	Description
1	Ground	Ground	20	Ground	Ground
2	Tx2n	Connected to lane Rx2 Inverted Data	21	Rx2n	Connected to lane Tx2 Inverted Data
3	Tx2p	Connected to lane Rx2 Non-Inverted Data	22	Rx2p	Connected to lane Tx2 Non-Inverted Data
4	Ground	Ground	23	Ground	Grounds
5	Not connected	Not connected	24	Not connected	Not connected
6	Not connected	Not connected	25	Not connected	Not connected
7	Ground	Ground	26	Ground	Ground
8	Mod-SelL	Cable Select	27	ModPrsL	Cable Present
9	ResetL	Cable Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power supply receiver	29	Vcc Tx	+3.3V Power supply transmitter
11	SCL	2-wire serial interface clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire serial interface data	31	LPMode	Low Power Mode
13	Ground	Ground	32	Ground	Ground
14	Not connected	Not connected	33	Not connected	Not connected
15	Not connected	Not connected	34	Not connected	Not connected
16	Ground	Ground	35	Ground	Ground
17	Rx1p	Connected to lane Tx1 Non-Inverted Data	36	Tx1p	Connected to lane Rx1 Non-Inverted Data
18	Rx1n	Connected to lane Tx1 Inverted Data	37	Tx1n	Connected to lane Rx1 Inverted Data
19	Ground	Ground	38	Ground	Ground

QSFP56 Module Pad Layout



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Specifications

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Between the operational specifications and absolute maximum ratings, prolonged operation is not intended and permanent device degradation may occur.

Parameter	Min	Max	Max
Supply Voltage	-0.3	3.6	V
Data Input Voltage	-0.3	3.6	V
Control Input Voltage	-0.3	3.6	V

Environmental Specifications

This table shows the environmental specifications for the product.

Parameter	Min	Max	Units
Storage Temperature	-40	85	°C

Operational Specifications

This section shows the range of values for normal operation.

Parameter	Min	Typ	Max	Units
Supply Voltage (Vcc)	3.135	3.3	3.465	V
Power Consumption	--	--	0.1	W
Operating Case Temperature	0		70	°C
Operating Relative Humidity	5		85	%

Electrical Specifications

Parameter	Min	Typ	Max	Units	Note
Characteristic impedance	90	100	110	Ω	
Time propagation delay	--	--	4.5	ns/m	Informative

OSFP Memory Map

Page 00 Addr.	Register Name	Value and Description
0	SFF8024 Identifier	19h: OSFP form factor 8x pluggable transceiver
1	CMIS Revision Compliance	50h: CMIS Rev 5.0
2	Memory Model, MciMaxSpeed	80h: Flat memory (no paging), no CLEI, max 400 kHz TWI (I2C) frequency
3	Global status	07h: Module Ready, Interrupt not asserted
04 - 84	Lanes and flags	00h: No lane flags, no DDM flags
85	Media Type	03h: Passive Copper
86 - 117		Application Descriptors (8 x 4 bytes) numbered 1...8

Start Address	Application Descriptor	Host IF	Media IF	Host/Media Lane cnt	Host Lane Assignment
86 - 89	1	31h: InfiniBand NDR, 2 ports	01h: Copper Cable	22h: 4 host + 4 media	55h: Lane 1 and 5
90 - 93	2	2Ch: IB SDR (4x two ports)	01h	22h	55h
94 - 97	3	1Bh: Eth 800GBASE-CR8 (8x one port)	01h	22h	55h
98 - 101	4	18h: Eth 400GBASE-CR4 (4x two ports)	01h	11h	FFh
102 -105	5	45h: 200GBASE-CR2 (four ports)	01h	22h	55h
106 - 109	6	16h: 100GBASE-CR1 (eight ports)	01h	11h	FFh
110 -113	7	01h: 400GBASE-CR8 (one port)	01h	11h	FFh
114 - 117	8	FFh: 200GBASE-CR4 (two ports)	00h	00h	00h

118 - 121	Password Chg Entry	
122 - 125	Password Entry	
126	Bank Select Byte	
127	Page Select Byte	
128	SFF8024 Identifier	19h: OSFP form factor 8x pluggable transceiver (same as addr 00)
129 - 144	VendorName	Vendor name (ASCII), padded w spaces: 'NVIDIA '
145	VendorOUI	Nvidia OUI: 48h, B0h, 2Dh
148 - 163	VendorPN	Part number: 'MCP7Y70-HXXX'
164 - 165	VendorRev	Revision
166 - 181	VendorSN	Serial number
182 - 189	DateCode	Date code, (YYMMDD__)
200	Power Class	00h: Power Class 1, 07h: max power in units of 0.25 W
201	Max power consumption	01(in multiplier x 0.25W)

Page 00 Addr.	Register Name	Value and Description
202	Link Length	Cable Length (m), 7-6: multiplier x value in bits 5-0 (00 = multiplier of .1 \ 01 = multiplier of 1\10 = multiplier of 10 \11 = multiplier of 100), e.g. 41h: 1 m
203	Connector Type	Connector Type (SFF-8024) 23h: No separable connector
204 - 207	Attenuation	Cable attenuation at 5, 7, 12.9, 25.8 GHz
210	Media Lane Info	00h: all near end lanes are implemented
211	Far End Config.	0Ch: 4x applications with 8x lanes each (aa,cc,ee,gg)
212	Media IF Technology	0Ah: Copper cable, unequalized
222	PageChecksum	Checksum of bytes 128-221 (low order 8 bits)
223 - 255	Custom Info	Custom data including traceability info

QSFP56 Memory Map

Page 00h	Register Name	Description
0	Identifier	11h: QSFP+ or later with SFF-8636 or SFF-8436 management interface
1	Status	08h: Support for SFF-8436 Rev. 2.8 and 2.9
113	Far End and Near End Implementations	1Ch: far ends with 4 lanes implemented in each; Lanes 0-1 implemented on near end.
128	Identifier	11h: QSFP+ or later with SFF-8636 or SFF-8436 management interface
129	Extended Identifier	00h: Not supported
130	Connector	23h: No separable connector (cable assembly with no separable interfaces)
139	Code for Serial Encoding Algorithm	08h: PAM4
146	Length	Length in units of 1m
147	Device technology	A0h: Copper cable unequalized
148-163	Vendor name	Mellanox: ASCII
164	Extended Module Codes for IB	3Fh: Supports HDR/FDR/EDR/QDR/DDR/SDR
165-167	QSFP vendor IEEE number	00-02-C9: Mellanox OUI. (different from OSFP)
168-183	Part number	Part number per backshell label (ASCII)
184-185	Product revision	ZZ: Revision per backshell label (ASCII)
186-189	Attenuation	@2.5G @5.0G @7.0G @12.9G
190	Max case temperature	46h: Support for 70°C
192		40h: 200GBase CR
196-211	Serial number	MTYYWWTTZZZZZ: Serial number per backshell label (ASCII).
212-217	Date code	YYMMDD: Year YY, month MM, day DD.
222	Signaling rate	6Ah: Nominal baud rate per channel, units of 250 MBd.
236	Vendor Specific	Floating part of length in units of 10cm (example: 1.5m = 0x1 in byte146 + 0x05 in byte 236)

Page 00h	Register Name	Description
237	Wire gauge	Wire thickness information. 1Eh: 30AWG

Mechanical Specifications

Parameter	Value		Units
Diameter	30AWG: 7.2 ±0.03 26AWG: 8.9 ±0.03		mm
Length tolerance	length < 2 m	±25	mm
	length ≥ 2 m	±50	

Minimum Bend Radius

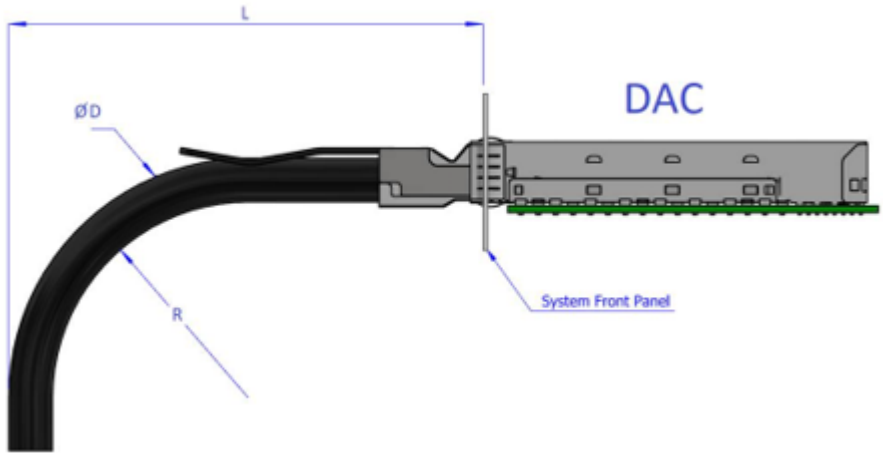
OPN	Length (m)	Cable Diameter	Min bend radius R (mm)	Assembly Space L** (mm)
MCP7Y70-H001	1.0	7.2	72	135
MCP7Y70-H01A	1.5	7.2	72	135
MCP7Y70-H002	2.0	8.9	89	156

The minimum assembly bending radius (close to the connector) is 10x the cable's outer diameter. The repeated bend (far from the connector) is also 10x the cable's outer diameter. The single bend (far from the connector) is 5x the cable's outer diameter.

**Combined end' is the 'head' where the cables join together, inserted into the switch. 'Single end' is the 'tail' which plugs into the HCA/NIC in a server.

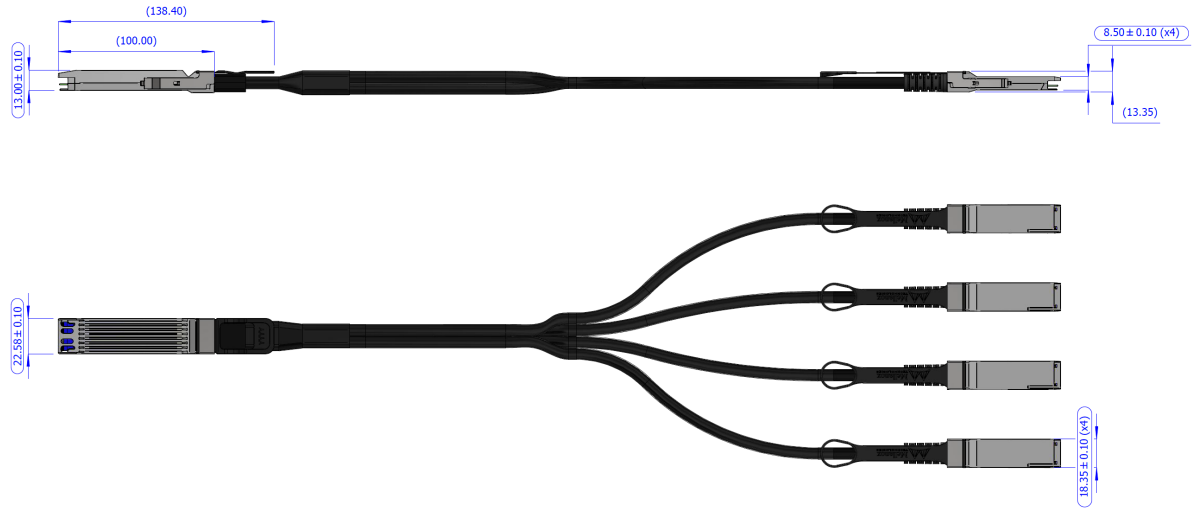
L = Assembly Space. Minimum value depends on the backshell (connector housing) dimensions = the space for the cable assembly behind the rack door.

Assembly Bending Radius

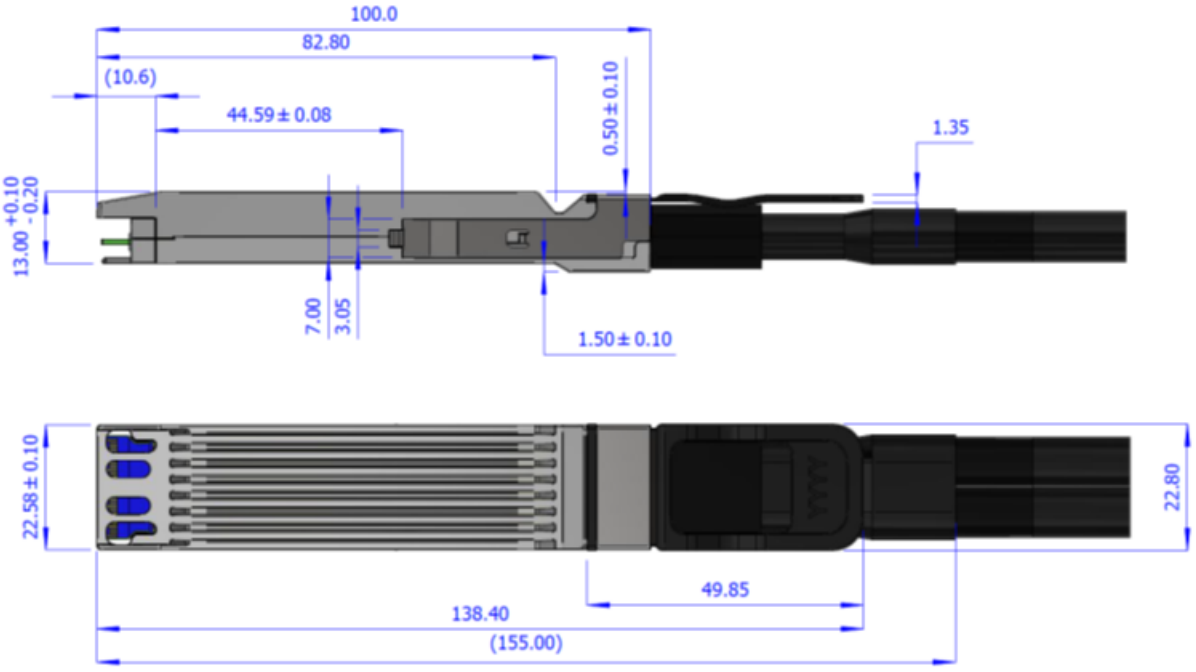


Mechanical Drawings

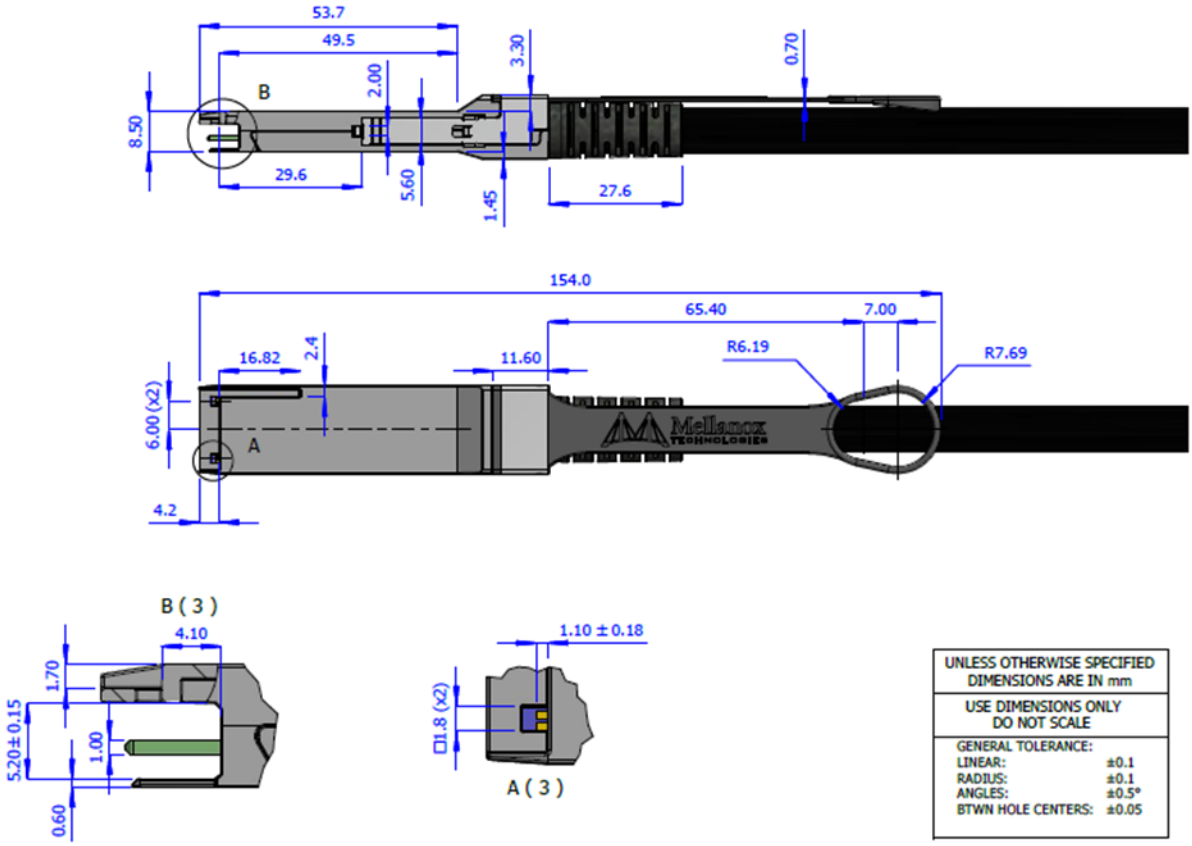
Dimensions



OSFP Finned Head Dimensions

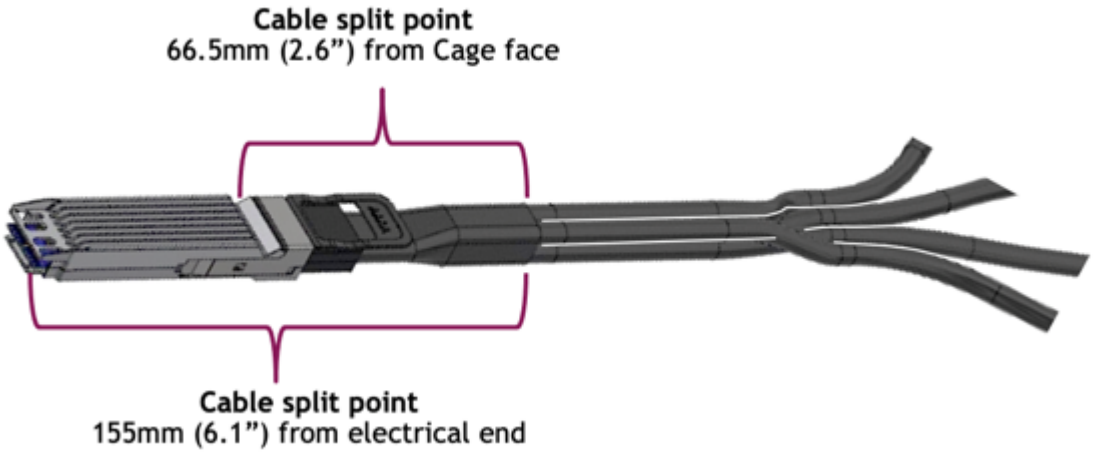


QSFP End Dimensions



Cable Length Definition (specified in Ordering Information section)

Cable Splitting Point



Labels

Backshell Label

The following label is applied on the cable’s backshell. Note that the images are for illustration purposes only. Labels look and placement may vary.

OSFP Head	QSFP56 Ends
Model No: MCP7Y70 PN: MCP7Y70-H01A SN: MTYYWWXXSSSSS Rev: A1 1.5m 30AWG YYYY-MM-DD 400Gb/s Made In COO	Model No: MCP7Y70 PN: MCP7Y70-H01A SN: MTYYWWXXSSSSS Rev: A1 1.5m 30AWG YYYY-MM-DD 100Gb/s Made In COO *(sample illustration)*

> ⚠ Images are for illustration purposes only. Product labels, colors, and form may vary.

Backshell Label Legend

Symbol	Meaning	Notes
PN - Part Number		

Symbol	Meaning	Notes
xx	Length	Meters
yy	Cable gauge	American wire gauge
SN - Serial Number		
MN	Manufacturer name	2 characters MT
YY	Year of manufacturing	2 digits
WW	Week of manufacturing	2 digits
MS	Manufacturer Site	2 characters
XXXXX	Serial number	5 digits for serial number. Reset at start of week to 00001.
Miscellaneous		
ZZ	HW and SW revision	2 alpha-numeric characters
Xm	Cable length	Meters
XXAWG	Cable gauge	American wire gauge
YYYY-MM-DD	Year-month-day	Year 4 digits, month 2 digits, day 2 digits
COO	Country of origin	E.g., China
	Quick response code	Serial number

Cable Jacket Label (Middle of Cable)

The following label is applied on the cable's jacket at each end. Note that the images are for illustration purposes only. Labels look and placement may vary.

(sample illustration)

> The serial number and barcode are for NVIDIA internal use only. Images are for illustration purposes only. Product labels, colors, and form may vary.

Regulatory Compliance and Classification

- Safety: CB, TUV, CE, EAC, UKCA
- EMC: CE, FCC, ICES, RCM, VCCI

Ask your NVIDIA FAE for a zip file of the certifications for this product.

FCC Class A Notice

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Cabling Information

Handling Precautions and Electrostatic Discharge (ESD)

The cable is compatible with ESD levels in typical data center operating environments and certified in accordance with the standards listed in the Regulatory Compliance Section. The product is shipped with protective caps on its connectors to protect it until the time of installation. In normal handling and operation of high-speed cables and optical transceivers, ESD is of concern during insertion into the QSFP cage of the server/switch. Hence, standard ESD handling precautions must be observed. These include use of grounded wrist/shoe straps and ESD floor wherever a cable/transceiver is extracted/inserted. Electrostatic discharges to the exterior of the host equipment chassis after installation are subject to system level ESD requirements.

Cable Management Guidelines

It is important to follow the instructions and information detailed NVIDIA Cable Management Guidelines and FAQ Application Note to insure proper and optimal installation of this cable and avoid physical damage.

Ordering Information

Ordering Part Number	Description
MCP7Y70-H001	NVIDIA passive copper splitter cable, IB twin port HDR 400Gb/s to 4x100Gb/s, OSFP to 4xQSFP56, 1m
MCP7Y70-H002	NVIDIA passive copper splitter cable, IB twin port HDR 400Gb/s to 4x100Gb/s, OSFP to 4xQSFP56, 2m
MCP7Y70-H01A	NVIDIA passive copper splitter cable, IB twin port HDR 400Gb/s to 4x100Gb/s, OSFP to 4xQSFP56, 1.5m

Document Revision History

Revision	Date	Description of Changes
1.2	Jun. 2023	Added Cable Length Definition to the Mechanical Specifications section.
1.1	Apr. 2023	Formatted and published in HTML.
1.0	Jan. 2022	Initial release. Preliminary and subject to change.

Notice

This document is provided for information purposes only and shall not be regarded as a warranty of a certain functionality, condition, or quality of a product. Neither NVIDIA Corporation nor any of its direct or indirect subsidiaries and affiliates (collectively: “NVIDIA”) make any representations or warranties, expressed or implied, as to the accuracy or completeness of the information contained in this document and assumes no responsibility for any errors contained herein. NVIDIA shall have no liability for the consequences or use of such information or for any infringement of patents or other rights of third parties that may result from its use. This document is not a commitment to develop, release, or deliver any Material (defined below), code, or functionality.

NVIDIA reserves the right to make corrections, modifications, enhancements, improvements, and any other changes to this document, at any time without notice. Customer should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

NVIDIA products are sold subject to the NVIDIA standard terms and conditions of sale supplied at the time of order acknowledgement, unless otherwise agreed in an individual sales agreement signed by authorized representatives of NVIDIA and customer (“Terms of Sale”). NVIDIA hereby expressly objects to applying any customer general terms and conditions with regards to the purchase of the NVIDIA product referenced in this document. No contractual obligations are formed either directly or indirectly by this document.

NVIDIA products are not designed, authorized, or warranted to be suitable for use in medical, military, aircraft, space, or life support equipment, nor in applications where failure or malfunction of the NVIDIA product can reasonably be expected to result in personal injury, death, or property or environmental damage. NVIDIA accepts no liability for inclusion and/or use of NVIDIA products in such equipment or applications and therefore such inclusion and/or use is at customer’s own risk.

NVIDIA makes no representation or warranty that products based on this document will be suitable for any specified use. Testing of all parameters of each product is not necessarily performed by NVIDIA. It is customer’s sole responsibility to evaluate and determine the applicability of any information contained in this document, ensure the product is suitable and fit for the application planned by customer, and perform the necessary testing for the application in order to avoid a default of the application or the product. Weaknesses in customer’s product designs may affect the quality and reliability of the NVIDIA product and may result in additional or different conditions and/or requirements beyond those contained in this document. NVIDIA accepts no liability related to any default, damage, costs, or problem which may be based on or attributable to: (i) the use of the NVIDIA product in any manner that is contrary to this document or (ii) customer product designs.

No license, either expressed or implied, is granted under any NVIDIA patent right, copyright, or other NVIDIA intellectual property right under this document. Information published by NVIDIA regarding third-party products or services does not constitute a license from NVIDIA to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property rights of the third party, or a license from NVIDIA under the patents or other intellectual property rights of NVIDIA.

Reproduction of information in this document is permissible only if approved in advance by NVIDIA in writing, reproduced without alteration and in full compliance with all applicable export laws and regulations, and accompanied by all associated conditions, limitations, and notices.

THIS DOCUMENT AND ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, “MATERIALS”) ARE BEING PROVIDED “AS IS.” NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY, OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE. TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL NVIDIA BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF NVIDIA HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Notwithstanding any damages that customer might incur for any reason whatsoever, NVIDIA’s aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms of Sale for the product.

Trademarks

NVIDIA, the NVIDIA logo, and Mellanox are trademarks and/or registered trademarks of NVIDIA Corporation and/or Mellanox Technologies Ltd. in the U.S. and in other countries. Other company and product names may be trademarks of the respective companies with which they are associated.