



**MFA7U10-H00x 400Gb/s OSFP to
2x200Gb/s QSFP56 HDR Active Optical
Splitter Cable**


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1 Introduction

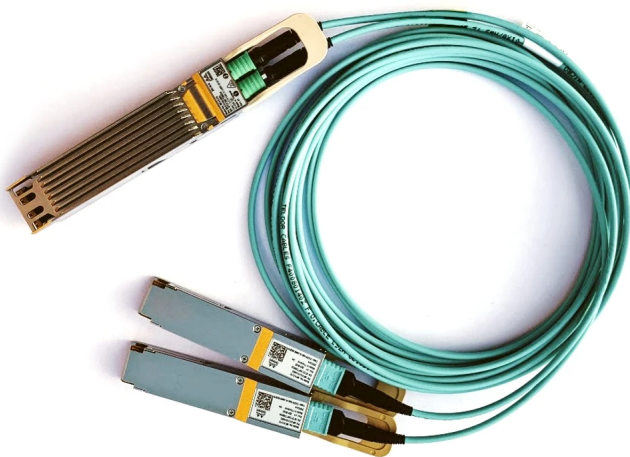
NVIDIA MFA7U10 is an OSFP to 2x QSFP56, 400Gb/s to 2 x 200Gb/s Active Optical splitter Cable (AOC) designed for connecting NVIDIA NDR and 400GbE Ethernet switches with OSFP cage, to legacy 2 HDR/200GbE switch/HCA QSFP56 cages.


The cable is compliant with SFF-8665 for the QSFP56 pluggable solution. It provides connectivity between system units with an OSFP 400Gb/s connector on one side and two separate QSFP56 200Gb/s connectors on the other side, such as a switch and two servers. The cable connects data signals from each of the 8 MMF (Multimode Fiber) pairs on the single OSFP end to the four pairs of each of the QSFP56 multiport ends. Each QSFP56 and OSFP end of the cable comprises an EEPROM providing product and status monitoring information, which can be read by the host system.

 Both Ethernet (ETH) and InfiniBand (IB) applications are supported only with ConnectX-6 cards.

Rigorous production testing ensures the best out-of-the-box installation experience, performance, and durability.

NVIDIA's unique quality active fiber cable solutions provide power-efficient connectivity for data center interconnects. It enables higher port bandwidth, density and configurability at a low cost, and reduced power requirement in the data centers.



 Images are for illustration purposes only. Product labels, colors, and lengths may vary.

1.1 Key Features

- 400Gb/s to 2x200Gb/s data rate
- Programmable Rx output amplitude and pre-emphasis
- OSFP head end is CMIS 4.0 compliant
- QSFP56 ends are SFF-8636 compliant

- Single 3.3V power supply
- 5W Max power consumption for QSFP56 ends
- 10W Max power consumption for the OSFP head end
- Hot pluggable
- RoHS compliant
- SFF-8636 compliant I²C management interface

2 Pin Description

The AOC is OSFP MSA Specification for OSFP Octal Small Form Factor Pluggable Module Rev. 1.12 compliant, see www.osfpmsa.org.

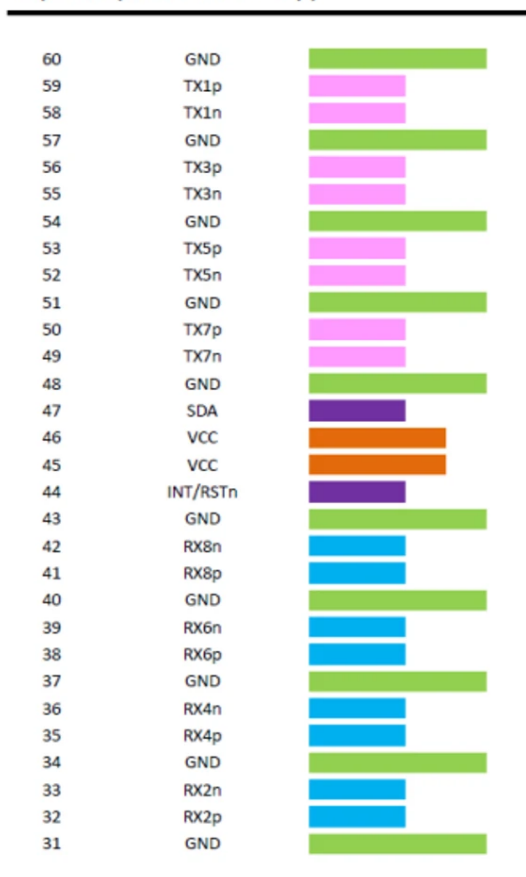
2.1 OSFP Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	31	GND	Ground
2	Tx2p	Transmitter Non-Inverted Data Input	32	Rx2p	Receiver Non-Inverted Data Output
3	Tx2n	Transmitter Inverted Data Input	33	Rx2n	Receiver Inverted Data Output
4	GND	Ground	34	GND	Grounds
5	Tx4p	Transmitter Non-Inverted Data Input	35	Rx4p	Receiver Non-Inverted Data Output
6	Tx4n	Transmitter Inverted Data Input	36	Rx4n	Receiver Inverted Data Output
7	GND	Ground	37	GND	Ground
8	Tx6p	Transmitter Non-Inverted Data Input	38	Rx6p	Receiver Non-Inverted Data Output
9	Tx6n	Transmitter Inverted Data Input	39	Rx6n	Receiver Inverted Data Output
10	GND	Ground	40	GND	Ground
11	Tx8p	Transmitter Non-Inverted Data input	41	Rx8p	Receiver Non-Inverted Data Output
12	Tx8n	Transmitter Inverted Data Input	42	Rx8n	Receiver Inverted Data Output
13	GND	Ground	43	GND	Ground
14	SCL	2-wire serial interface clock	44	INT / RSTn	Module Interrupt / Module Reset
15	VCC	+3.3V Power	45	VCC	+3.3V Power
16	VCC	+3.3V Power	46	VCC	+3.3V Power
17	LPWn / PRSn	Low-Power Mode / Module Present	47	SDA	2-wire Serial interface data
18	GND	Ground	48	GND	Ground
19	Rx7n	Receiver Inverted Data Output	49	Tx7n	Transmitter Inverted Data Input
20	Rx7p	Receiver Non-Inverted Data Output	50	Tx7p	Transmitter Non-Inverted Data Input
21	GND	Ground	51	GND	Ground
22	Rx5n	Receiver Inverted Data Output	52	Tx5n	Transmitter Inverted Data Input

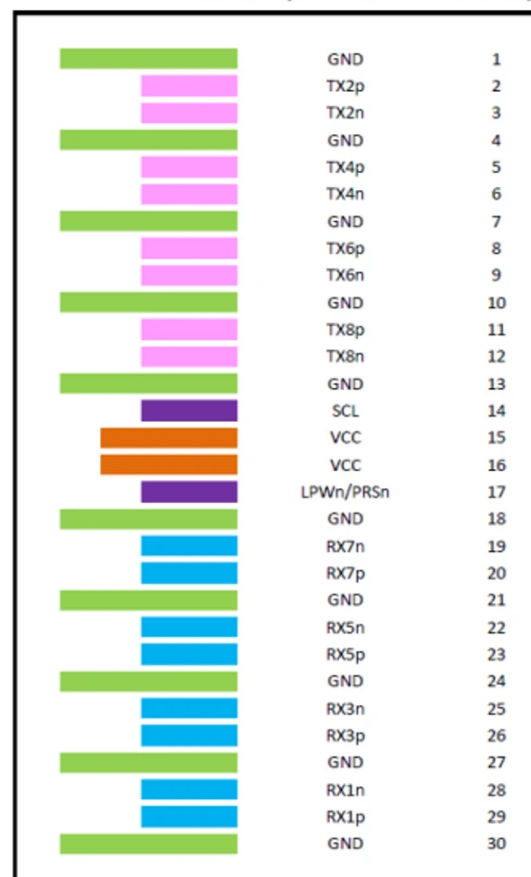
Pin	Symbol	Description	Pin	Symbol	Description
23	Rx5p	Receiver Non-Inverted Data Output	53	Tx5p	Transmitter Non-Inverted Data Input
24	GND	Ground	54	GND	Ground
25	Rx3n	Receiver Inverted Data Output	55	Tx3n	Transmitter Inverted Data Input
26	Rx3p	Receiver Non-Inverted Data Output	56	Tx3p	Transmitter Non-Inverted Data Input
27	GND	Ground	57	GND	Ground
28	Rx1n	Receiver Inverted Data Output	58	Tx1n	Transmitter Inverted Data Input
29	Rx1p	Receiver Non-Inverted Data Output	59	Tx1p	Transmitter Non-Inverted Data Input
30	GND	Ground	60	GND	Ground

2.1.1 OSFP Module Pad Layout

Top Side (viewed from top)



Bottom Side (viewed from bottom)



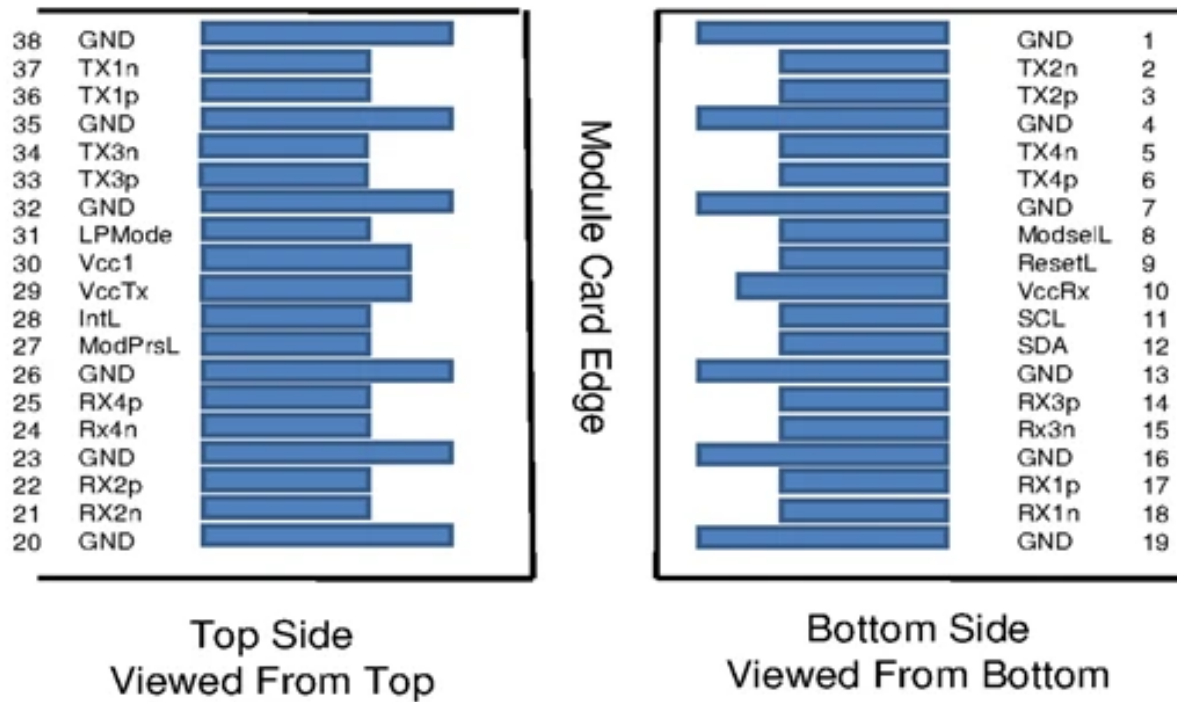
----- Module Card Edge -----

The Active Optical Cable (AOC) pin assignment is SFF-8679 compliant.

2.2 QSFP56 Pin Description 200Gb/s End

Pin	Symbol	Description	Pin	Symbol	Description
1	Ground	Ground	20	Ground	Ground
2	Tx2n	Connected to Port 1 lane Rx2 Inverted Data	21	Rx2n	Connected to Port 1 lane Tx2 Inverted Data
3	Tx2p	Connected to Port 1 lane Rx2 Non-Inverted Data	22	Rx2p	Connected to Port 1 lane Tx2 Non-Inverted Data
4	Ground	Ground	23	Ground	Grounds
5	Tx4n	Connected to Port 2 lane Rx2 Non-Inverted Data	24	Rx4n	Connected to Port 2 lane Tx2 Inverted Data
6	Tx4p	Connected to Port 2 lane Rx2 Inverted Data	25	Rx4p	Connected to Port 2 lane Tx2 Non-Inverted Data
7	Ground	Ground	26	Ground	Ground
8	Mod-Sell	Cable Select	27	ModPrsL	Cable Present
9	ResetL	Cable Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power supply receiver	29	Vcc Tx	+3.3V Power supply transmitter
11	SCL	2-wire serial interface clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire serial interface data	31	LPMode	Low Power Mode
13	Ground	Ground	32	Ground	Ground
14	Rx3p	Connected to Port 2 lane Tx1 Non-Inverted Data	33	Tx3p	Connected to Port 2 lane Rx1 Non-Inverted Data
15	Rx3n	Connected to Port 2 lane Tx1 Inverted Data	34	Tx3n	Connected to Port 2 lane Rx1 Inverted Data
16	Ground	Ground	35	Ground	Ground
17	Rx1p	Connected to Port 1 lane Tx1 Non-Inverted Data	36	Tx1p	Connected to Port 1 lane Rx1 Non-Inverted Data
18	Rx1n	Connected to Port 1 lane Tx1 Inverted Data	37	Tx1n	Connected to Port 1 lane Rx1 Inverted Data
19	Ground	Ground	38	Ground	Ground

2.2.1 QSFP56 Module Pad Layout



2.3 Control Signals (OSFP)

This AOC has CMIS 4.0 (check for update, e.g. to CMIS 5) compliant management interface and OSFP 4.1 (check for update) compliant form factor and interfaces. This implies that the control signals shown in the pad layout are implemented with the following functions:

Name	Function	Description
LPWn/PRSn	Input/output	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification [].
INT/RSTn	Input, /output	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in the OSFP Specification [].
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	Bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.

2.4 Control Signals (QSFP)

This AOC is SFF-8636 compliant. This means that the control signals shown in the pad layout support the following functions:

Name	Function	Description
ModPrsL	Output	Module Present pin, grounded inside the module. Terminated with pull-up in the host system. Asserted low when the transceiver is inserted, whereby the host detects the presence of the transceiver.
ModSelL	Input	Module Select, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.
ResetL	Input	Reset, pulled high in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_{Reset_init}) initiates a complete module reset, returning all user module settings to their default state. During reset the host shall disregard all status bits until the module indicates completion of the reset interrupt by asserting IntL signal low with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module completes the reset interrupt without requiring a reset.
LPMODE	Input	Low Power Mode input, pulled up inside the module. The transceiver starts up in low power mode, i.e. <1.5 W with the two-wire interface active. The host system can read the power class declaration from the transceiver and determine if it has enough power to enable the high-speed operation/high power mode of the transceiver. This can be done by asserting LPMODE low or by use of the Power_override and Power_set control bits (Address A0h, byte 93 bits 0,1).
IntL	OC output	Interrupt Low, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’.
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	Bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.

The low-speed signals are Low Voltage TTL (LVTTTL) compliant (except for SCL and SDA signals).

2.5 Diagnostics and Other Features

The AOC complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis

- Tx/Rx CDR control
by default enabled for 100 GbE operation, disable it for 40G operation

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the SFF-8636 MSA.

3 Specifications

3.1 Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

3.1.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply voltage	-0.3	3.6	V
Data input voltage	-0.3	3.465	V
Control input voltage	-0.3	4.0	V
Damage Threshold	3.4	---	dBm

3.1.2 Environmental Specifications

This table shows the environmental specifications for the product.

Parameter	Min	Max	Units
Storage temperature	-40	85	°C

3.1.3 Operational Specifications

This section shows the range of values for normal operation. The host board power supply filtering should be designed as recommended in the SFF Committee Spec.

Parameter	Min	Typ	Max	Units	Notes
Supply voltage (V_{CC})	3.135	3.3	3.465	V	---
Power consumption 200Gb/s end	---	4.35	4.5	W	---
Power consumption 400Gb/s end	---	9.0	10	W	---
Supply noise tolerance (10Hz - 10MHz)	66	---	---	mVpp	---
Operating case temperature	0	---	70	°C	---
Operating relative humidity	5	---	85	%	---

3.1.4 Electrical Specifications

Parameter (per lane)	Min	Typ	Max	Units
Signaling rate	-100 ppm	26.5625	+100 ppm	GBd
Differential data input swing at TP1a	TBD	---	900	mVpp
Differential data output swing at TP4	---	---	900	mVpp
Near-end ESMW	0.265	---	---	UI
Near-end output eye height	70	---	---	mVpp
Output transition time, 20% to 80%	9.5	---	---	ps

Notes:

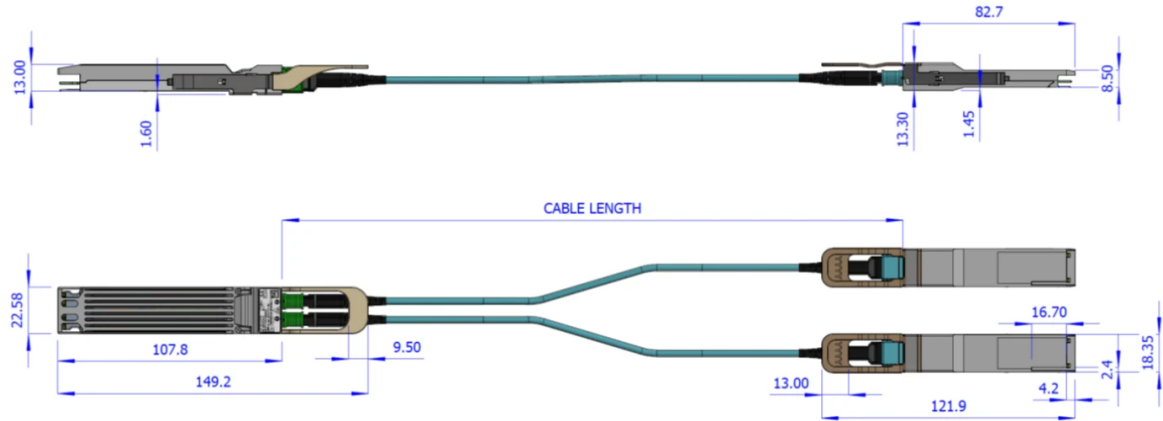
- Multiple clock domains are supported only on line-side Rx.
- QSFP Tx CDR lock can only occur if Tx lane 4 is transmitting data.

3.1.5 Mechanical Specifications

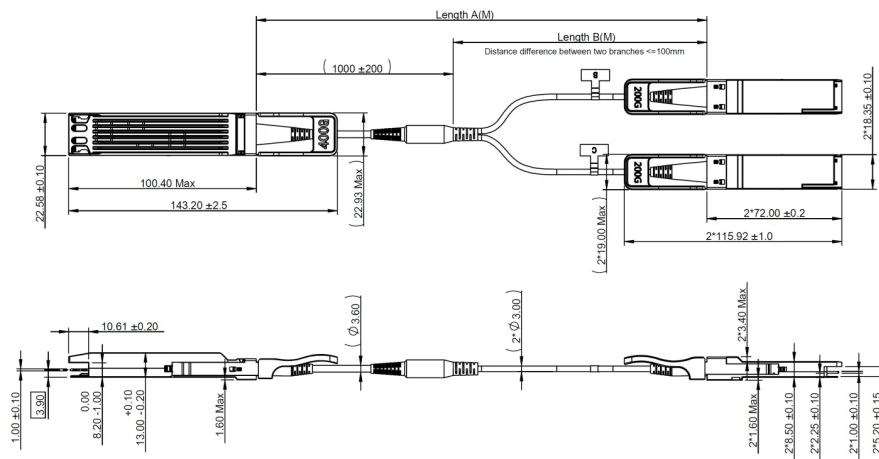
Parameter	Value		Units
Diameter	3 +/-0.2		mm
Minimum bend radius	30		mm
Length tolerance	length < 5 m	+300 / -0	mm
	5 m ≤ length < 50 m	+500 / -0	
	50 m ≤ length	+1000 / -0	
Cable color	Aqua		---
Cable Jacket	LSZH/OFNR		---

3.1.5.1 Mechanical Dimensions

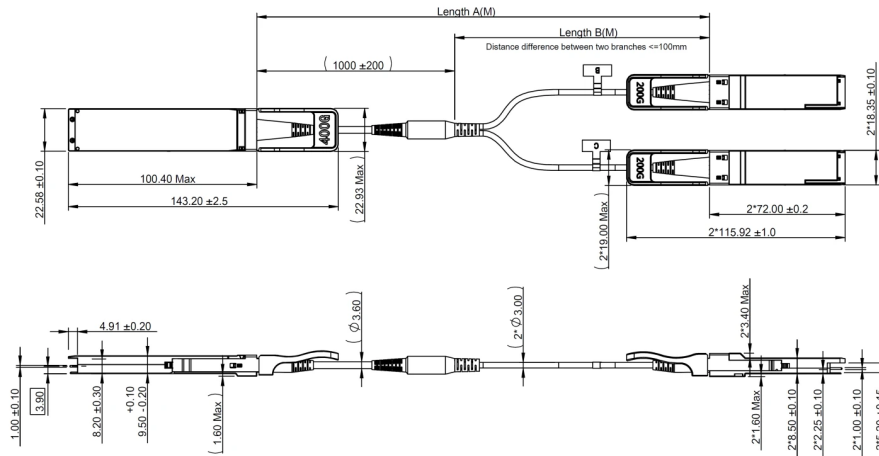
3.1.5.1.1 Option 1



3.1.5.1.2 Option 2



3.1.5.1.3 Option 3



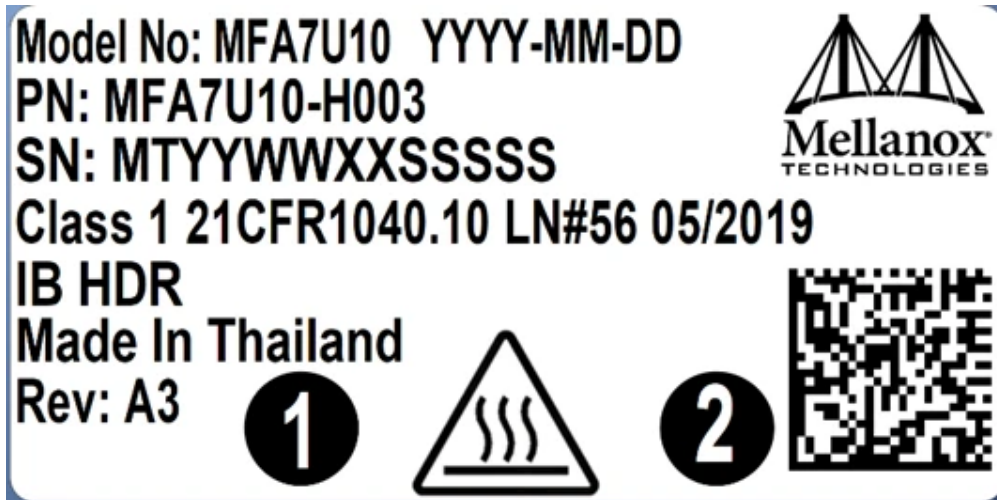
3.1.5.2 Connectivity Schematic

400Gb/s Side	2x200Gb/s Side
	Port 1
TX1	RX1
RX1	TX1
TX2	RX2
RX2	TX2
TX3	RX3
RX3	TX3
TX4	RX4
RX4	TX4
	Port 2
TX5	RX1
RX5	TX1
TX6	RX2
RX6	TX2
TX7	RX3
RX7	TX3
TX8	RX4
RX8	TX4

3.2 Labels

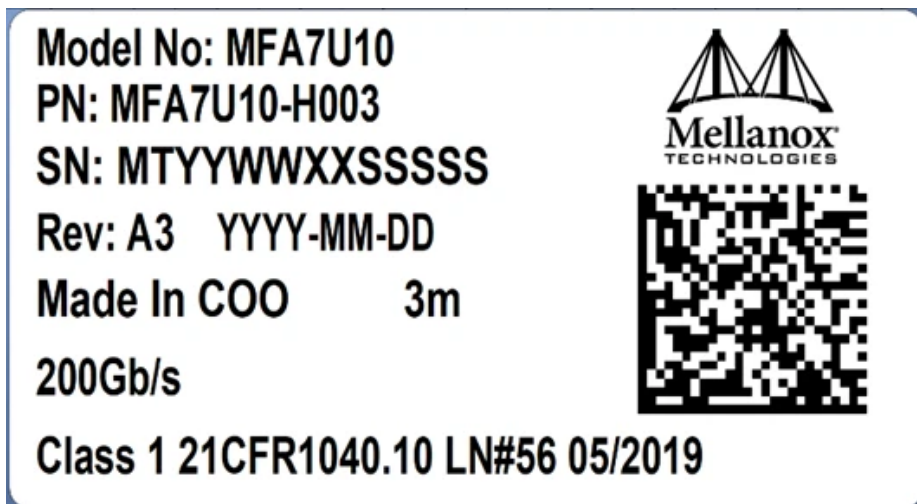
The following labels are applied on the AOC backshells:

3.2.1 400Gb/s Backshell Label



(sample illustration)

3.2.2 200Gb/s Backshell Label



(sample illustration)

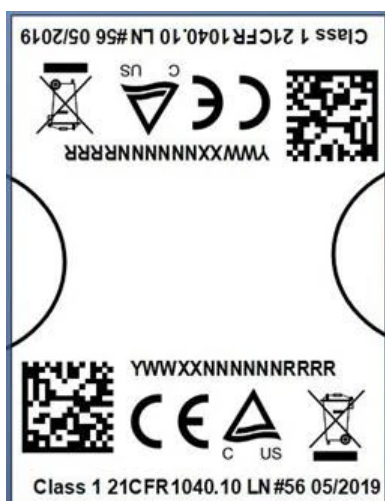
3.2.3 Backshell Label Legend

Symbol	Meaning	Notes
PN - Part Number		
xx	Length	Meter

Symbol	Meaning	Notes
SN - Serial Number		
MT	Manufacturer name	2 characters, e.g. MT
YY	Year of manufacturing	2 digits
WW	Week of manufacturing	2 digits
XX	Manufacturer site	2 characters
SSSSS	Serial number	5 digits for serial number, starting from 00001. Reset at start of week to 00001.
Miscellaneous		
ZZ	HW and SW revision	2 alpha-numeric characters
YYYY	Year of manufacturing	4 digits
MM	Month of manufacturing	2 digits
DD	Day of manufacturing	2 digits
COO	Country of origin	E.g. China or Malaysia
XXm	Cable length	Meter
<input type="checkbox"/>	Quick response code	Serial number (MTYYWWXXSSSSS)

The following label is applied on the cable's jacket:

3.2.4 Fiber Cable Jacket Label



(sample illustration)

Note: The serial number and barcode are for NVIDIA internal use only.

3.2.5 Splitter Cable Labels Identifying the 2 QSFP56 Tails



(sample illustration)

3.3 Regulatory Compliance and Classification

The laser module is classified as class I according to IEC 60825-1, IEC 60825-2 and 21 CFR 1040 (CDRH).

- Safety: CB, cTUVus, CE
- EMC: CE, FCC, ICES, RCM, VCCI

Ask your NVIDIA FAE for a zip file of the certifications for this product.

3.4 FCC Class A Notice

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.



3.5 Handling Precautions and Electrostatic Discharge (ESD)

The MFA7U10 is compatible with ESD levels in typical data center operating environments and certified in accordance with the standards listed in the Regulatory Compliance Section. The product is shipped with protective caps on its connectors to protect it until the time of installation. In normal handling and operation of high-speed cables and optical transceivers, ESD is of concern during insertion into the QSFP cage of the server/switch. Hence, standard ESD handling precautions must be observed. These include use of grounded wrist/shoe straps and ESD floor wherever a cable/transceiver is extracted/inserted. Electrostatic discharges to the exterior of the host equipment chassis after installation are subject to system level ESD requirements.

4 Ordering Information

Ordering Part Number	Description
MFA7U10-H003	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 3m
MFA7U10-H005	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 5m
MFA7U10-H010	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 10m
MFA7U10-H015	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 15m
MFA7U10-H020	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 20m
MFA7U10-H030	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 30m
MFA7U10-H003-FLT	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 3m flat top
MFA7U10-H005-FLT	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 5m flat top
MFA7U10-H010-FLT	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 10m flat top
MFA7U10-H015-FLT	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 15m flat top
MFA7U10-H020-FLT	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 20m flat top
MFA7U10-H030-FLT	NVIDIA AOC splitter, IB twin port HDR, 400Gb/s to 2x200Gb/s, OSFP to 2xQSFP56, 30m flat top

Refer [here](#) for the cable length definition.

5 References

- [NVIDIA_Cable_Management_Guidelines_and_FAQs_Application_Note \(MLNX-15-3603\)](#)

For documentation, please contact your sales representative or the Support team.

6 Document Revision History

Revision	Date	Description
1.4	Apr. 2024	Updated the Introduction page.
1.3	Jan. 2024	Updated mechanical drawings and the OPNs in the Ordering Information section.
1.2	Oct. 2023	Updated Mechanical Specifications to include Cable Jacket LSZH compliance.
1.1	May. 2023	Updated the Introduction and Specifications chapters.
1.0	Jan. 2022	Initial First release; preliminary and subject to change.

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