MFS1S50-V0xxE 200GbE QSFP56 to 2x100GbE QSFP56 MMF AOC Product Specifications

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Introduction

The NVIDIA® MFS1S50 is a QSFP56 VCSEL-based (Vertical Cavity Surface-Emitting Laser), cost-effective 200GbE to 2x 100GbE active optical splitter cable (AOC) designed for use in 200GbE Ethernet systems.

The MFS1S50 cable is compliant with SFF-8665 for the QSFP56 pluggable solution. It provides connectivity between system units with a 200GbE connector on one side and two separate 100GbE connectors on the other side, such as a switch and two servers. The cable connects data signals from each of the 4 MMF (Multi Mode Fiber) pairs on the single QSFP56 end to the dual pair of each of the QSFP56 multiport ends. Each QSFP56 end of the cable contains an EEPROM providing product and status monitoring information, which can be read by the host system.

NVIDIA's unique-quality cable solutions provide power-efficient connectivity for data center interconnects. It enables higher port bandwidth, density and configurability at a low cost, and reduced power requirement in the data centers. Rigorous production testing ensures the best out-of-the-box installation experience, performance and durability.

⚠ Images are for illustration purposes only. Product labels, colors, and lengths may vary.

Key Features

- 200GbE to 2x 100GbE data rate
- 4x 50Gb/s PAM4 modulation
- Programmable Rx output amplitude and pre-emphasis
- SFF-8665 compliant QSFP56 port
- Single 3.3V power supply
- 4.5W power consumption (typ., 200G end)
- Up to 30m length
- Hot pluggable
- RoHS compliant
- IEEE 802.3 200GBASE-SR4, and 100GBASE-SR2 compliant
- SFF-8636 compliant I^2C management interface

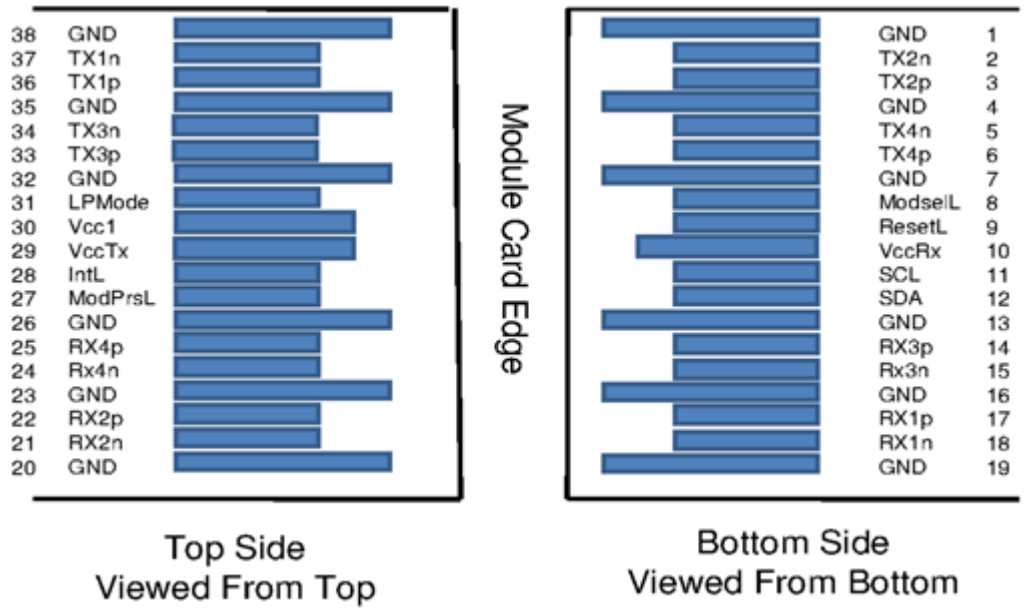
Pin Descriptions

The Active Optical Cable (AOC) pin assignment is SFF-8679 compliant.

QSFP56 Pin Description 200GbE End

Pin	Symbol	Description	Pin	Symbol	Description
1	Ground	Ground	20	Ground	Ground
2	Tx2n	Connected to Port 1 lane Rx2 Inverted Data	21	Rx2n	Connected to Port 1 lane Tx2 Inverted Data
3	Tx2p	Connected to Port 1 lane Rx2 Non-Inverted Data	22	Rx2p	Connected to Port 1 lane Tx2 Non-Inverted Data
4	Ground	Ground	23	Ground	Grounds
5	Tx4n	Connected to Port 2 lane Rx2 Non-Inverted Data	24	Rx4n	Connected to Port 2 lane Tx2 Inverted Data
6	Tx4p	Connected to Port 2 lane Rx2 Inverted Data	25	Rx4p	Connected to Port 2 lane Tx2 Non-Inverted Data
7	Ground	Ground	26	Ground	Ground
8	Mod-SelL	Cable Select	27	ModPrsL	Cable Present
9	ResetL	Cable Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power supply receiver	29	Vcc Tx	+3.3V Power supply transmitter
11	SCL	2-wire serial interface clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire serial interface data	31	LPMode	Low Power Mode
13	Ground	Ground	32	Ground	Ground
14	Rx3p	Connected to Port 2 lane Tx1 Non-Inverted Data	33	Tx3p	Connected to Port 2 lane Rx1 Non-Inverted Data
15	Rx3n	Connected to Port 2 lane Tx1 Inverted Data	34	Tx3n	Connected to Port 2 lane Rx1 Inverted Data
16	Ground	Ground	35	Ground	Ground
17	Rx1p	Connected to Port 1 lane Tx1 Non-Inverted Data	36	Tx1p	Connected to Port 1 lane Rx1 Non-Inverted Data
18	Rx1n	Connected to Port 1 lane Tx1 Inverted Data	37	Tx1n	Connected to Port 1 lane Rx1 Inverted Data
19	Ground	Ground	38	Ground	Ground

QSFP56 Module Pad Layout



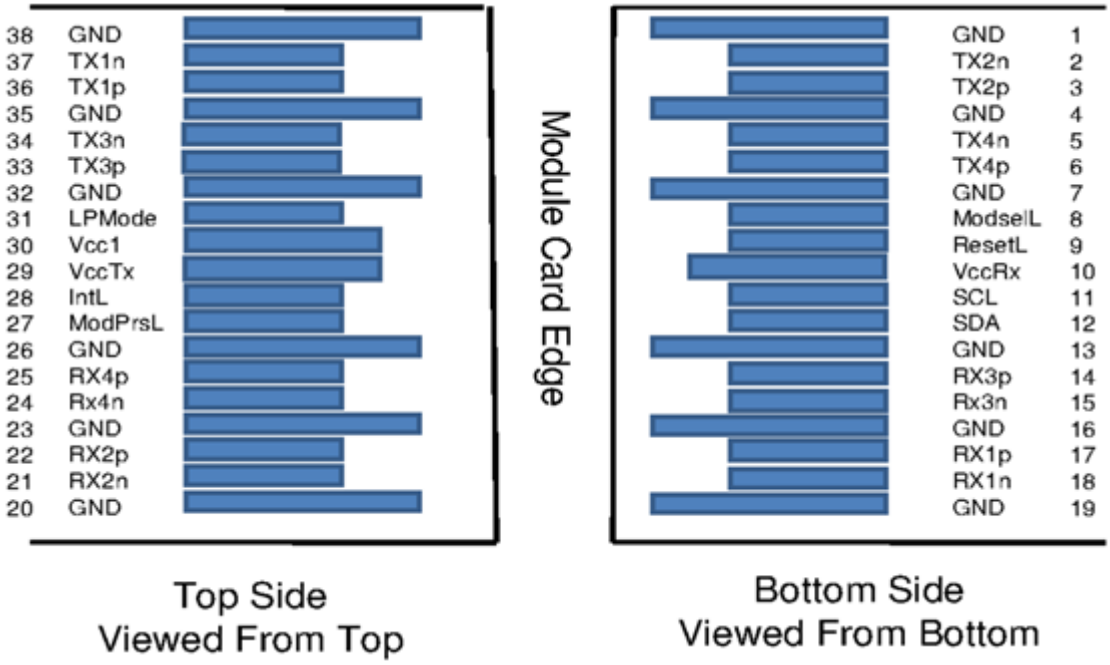
QSFP56 Pin Description 100GbE End

Pin	Symbol	Description	Pin	Symbol	Description
1	Ground	Ground	20	Ground	Ground
2	Tx2n	Connected to lane Rx2 Inverted Data	21	Rx2n	Connected to lane Tx2 Inverted Data
3	Tx2p	Connected to lane Rx2 Non-Inverted Data	22	Rx2p	Connected to lane Tx2 Non-Inverted Data
4	Ground	Ground	23	Ground	Grounds
5	Not connected	Not connected	24	Not connected	Not connected
6	Not connected	Not connected	25	Not connected	Not connected
7	Ground	Ground	26	Ground	Ground
8	Mod-SelL	Cable Select	27	ModPrsL	Cable Present
9	ResetL	Cable Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power supply receiver	29	Vcc Tx	+3.3V Power supply transmitter
11	SCL	2-wire serial interface clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire serial interface data	31	LPMode	Low Power Mode
13	Ground	Ground	32	Ground	Ground
14	Not connected	Not connected	33	Not connected	Not connected
15	Not connected	Not connected	34	Not connected	Not connected
16	Ground	Ground	35	Ground	Ground

Pin	Symbol	Description	Pin	Symbol	Description
17	Rx1p	Connected to lane Tx1 Non-Inverted Data	36	Tx1p	Connected to lane Rx1 Non-Inverted Data
18	Rx1n	Connected to lane Tx1 Inverted Data	37	Tx1n	Connected to lane Rx1 Inverted Data
19	Ground	Ground	38	Ground	Ground

QSFP56 Module Pad Layout

The pinout of the 100GbE ends of the cable is identical to the 200GbE end except that RF lanes 3 and 4 (pins 5, 6, 14, 15, 24, 25, 33, 34) are not used.



Digital Diagnostics

The transceiver complies with the SFF 8665 specification and has the following key features:

- Physical layer link optimization:
  - Programmable Rx output amplitude
  - Programmable Rx output pre-emphasis
- Digital Diagnostic Monitoring (DDM):
  - Rx receive optical power monitor
  - Tx transmit optical power monitor
  - Tx bias current monitor
  - Supply voltage monitor
  - Transceiver case temperature monitor

- Other SFF-8636 functions and interrupt indications:
    - Tx & Rx LOS indication
    - Tx & Rx LOL indication

Specifications

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.
Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Parameter	Min	Max	Units
Supply voltage	-0.3	3.6	V
Data input voltage	-0.3	3.465	V
Control input voltage	-0.3	4.0	V
Damage Threshold	3.4	---	dBm

Environmental Specifications

This table shows the environmental specifications for the product.

Parameter	Min	Max	Units
Storage temperature	-40	85	°C

Operational Specifications

This section shows the range of values for normal operation. The host board power supply filtering should be designed as recommended in the SFF Committee Spec.

Parameter	Min	Typ	Max	Units
Supply voltage (V_{CC})	3.135	3.3	3.465	V
Power consumption 200GbE end	---	4.5	5.0	W
Power consumption 100GbE end	---	3.0	3.5	W
Supply noise tolerance (10Hz – 10MHz)	66	---	---	mVpp
Operating case temperature	0	---	70	°C
Operating relative humidity	5	---	85	%

Electrical Specifications

Parameter (per lane)	Min	Typ	Max	Units
Signaling rate	-100 ppm	53.125	+100 ppm	GBd
Differential data input swing at TP1a	TBD	---	900	mVpp

Parameter (per lane)	Min	Typ	Max	Units
Differential data output swing at TP4	---	---	900	mVpp
Near-end ESMW	0.265	---	---	UI
Near-end output eye height	70	---	---	mVpp
Output transition time, 20% to 80%	9.5	---	---	ps

Notes:

- Multiple clock domains are supported only on line-side Rx. Host side Rx supports a single clock domain only.
- QSFP Tx CDR lock can only occur if Tx lane 4 is transmitting data.

Interoperability

For configurations tested with the AOCs please refer to the system level product (SLP) qualification report.

Digital Diagnostic Monitoring

The DDM functions are implemented according to SFF-8636 for reading the following key parameters with associated warning and alarm thresholds:

- Temperature with warning/alarm
- Supply voltage with warning/alarm
- Laser bias current with warning/alarm
- Transmitted optical power with warning/alarm
- Received optical power with warning/alarm

Rate Select

The AOC supports rate select, which is controlled by writing to registers 0x57-0x58. Two bits are assigned for each receiver lane in byte 0x57 (87dec, Rxn_Rate_Select) and two bits for each transmitter lane in byte 0x58 (88dec, Txn_Rate_Select) to specify up to four bitrates, as defined in SFF-8636 Rev 2.9.2 Table 6-5 XN_RATE_SELECT ENCODINGS. All four lanes are required to have the same rate select value.

The below table specifies the rate for each rate select setting.

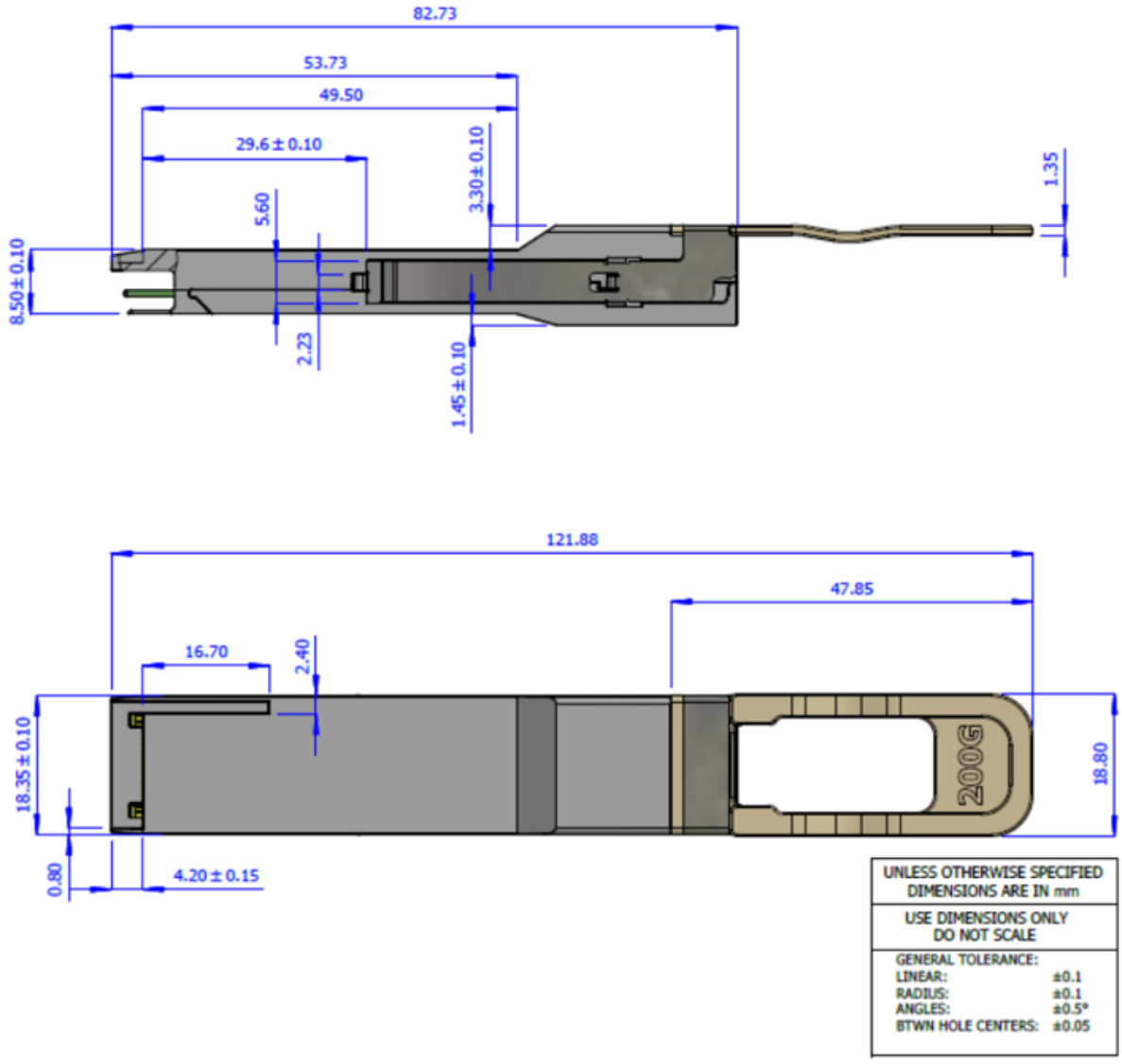
Rate Select Encodings

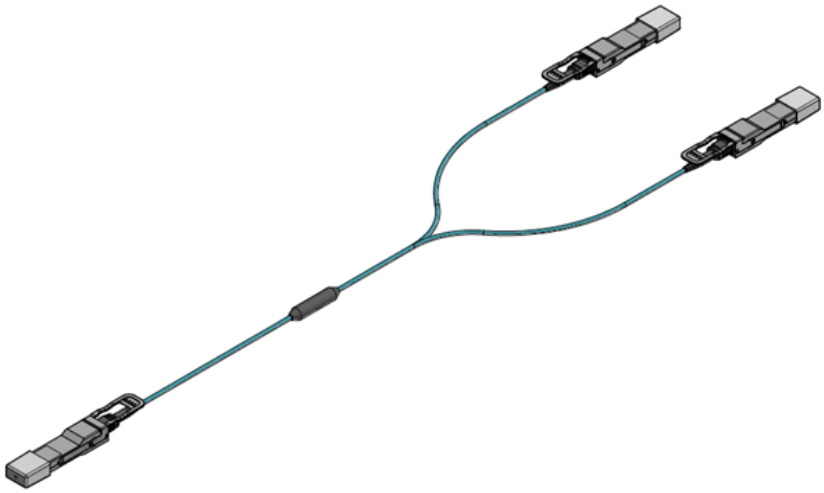
Rate Select Value	Operating Rate (GBd)
00	2.500000 NRZ
01	10.31250 NRZ
10	25.78125 NRZ
11	26.56250 PAM4

Mechanical Specifications

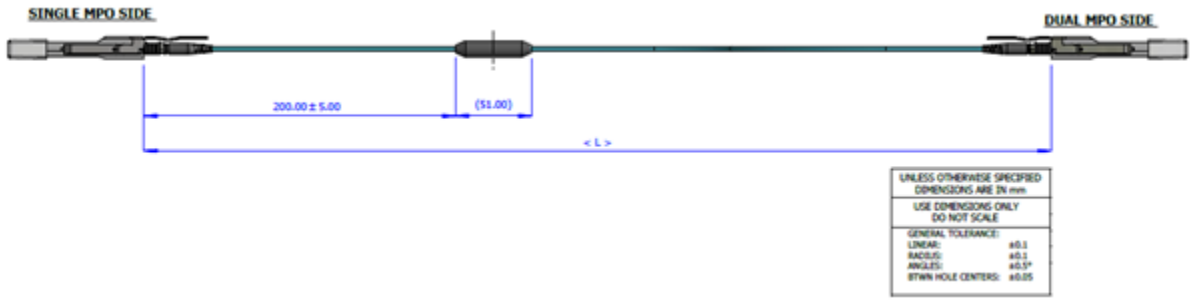
Parameter	Value		Units
Diameter	3 +/-0.2		mm
Minimum bend radius	30		mm
Length tolerance	length < 5 m	+300 /-0	mm
	5 m ≤ length < 50 m	+500 / -0	
	50 m ≤ length	+1000 /-0	
Cable color	Aqua		---

Mechanical Dimensions





Splicing Point and Cable Length



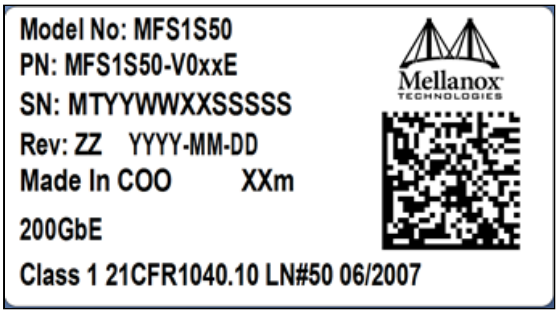
Connectivity Schematic

200GbE Side	2x100GbE Side
	Port 1
TX1	RX1
RX1	TX1
TX2	RX2
RX2	TX2
	Port 2
TX3	RX1
RX3	TX1
TX4	RX2
RX4	TX2

Labels

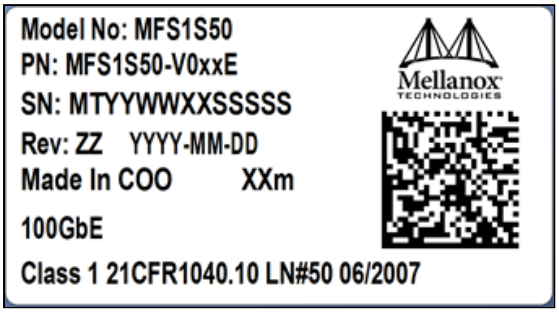
The following labels are applied on the AOC backshells:

200GbE Backshell Label



(sample illustration)

100GbE Backshell Label



(sample illustration)

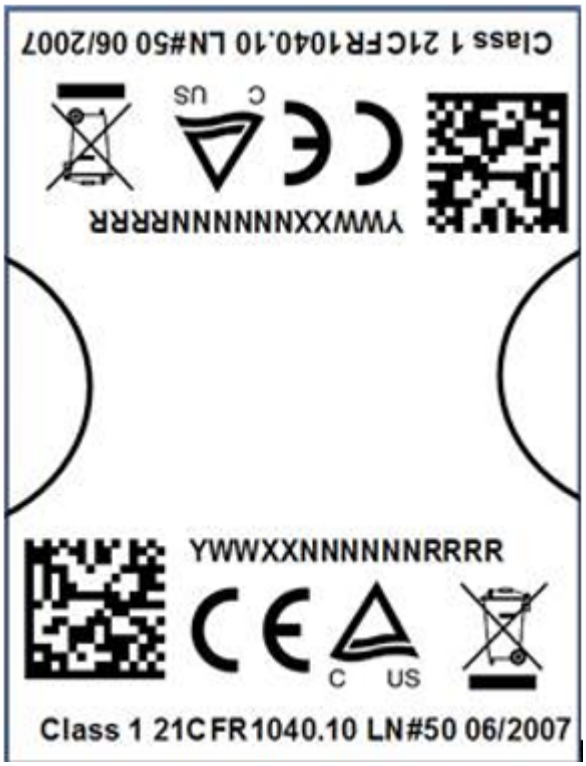
Backshell Label Legend

Symbol	Meaning	Notes
SN – Serial Number		
xx	Length	Meter
SN – Serial Number		
MT	Manufacturer name	2 characters, e.g. MT
YY	Year of manufacturing	2 digits
WW	Week of manufacturing	2 digits
XX	Manufacturer site	2 characters
SSSSS	Serial number	5 digits for serial number, starting from 00001. Reset at start of week to 00001.
Miscellaneous		
ZZ	HW and SW revision	2 alpha-numeric characters
YYYY	Year of manufacturing	4 digits
MM	Month of manufacturing	2 digits
DD	Day of manufacturing	2 digits
COO	Country of origin	E.g. China or Malaysia

Symbol	Meaning	Notes
XXm	Cable length	Meter
	Quick response code	Serial number (MTYYWWXXSSSSS)

The following label is applied on the cable's jacket:

Fiber Cable Jacket Label



(sample illustration)

Note: The serial number and barcode are for NVIDIA internal use only.

Splitter Cable Labels Identifying the 2 QSFP56 Tails

(sample illustration)

Regulatory Compliance and Classification

The laser module is classified as class I according to IEC 60825-1, IEC 60825-2 and 21 CFR 1040 (CDRH).

- Safety: CB, cTUVus, CE

- EMC: CE, FCC, ICES, RCM, VCCI

Ask your NVIDIA FAE for a zip file of the certifications for this product.

FCC Class A Notice

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Ordering Information

Ordering Part Number	Description
MFS1S50-V003E	Active fiber cable, 200GbE, 200Gb/s, QSFP56, LSZH, 3m
MFS1S50-V005E	Active fiber cable, 200GbE, 200Gb/s, QSFP56, LSZH, 5m
MFS1S50-V010E	Active fiber cable, 200GbE, 200Gb/s, QSFP56, LSZH, 10m
MFS1S50-V015E	Active fiber cable, 200GbE, 200Gb/s, QSFP56, LSZH, 15m
MFS1S50-V020E	Active fiber cable, 200GbE, 200Gb/s, QSFP56, LSZH, 20m
MFS1S50-V030E	Active fiber cable, 200GbE, 200Gb/s, QSFP56, LSZH, 30m

Refer here for the cable length definition.

References

1. LinkX_Memory_Map_Application_Note (MLNX-15-5926)
2. NVIDIA_Cable_Management_Guidelines_and_FAQs_Application_Note (MLNX-15-3603)

For documentation, please contact your sales representative or the Support team.

Document Revision History

Revision	Date	Description
1.2	Nov. 2021	Reformatted and rebranded; migrated to HTML. Removed BER bullet.
1.1	Dec. 5, 2018	Inserted watermark disclaimer.
1.0	Nov. 29, 2018	Initial revision

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