MMA1L10-CR 100GbE QSFP28 LR4 Transceiver Product Specifications

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Introduction

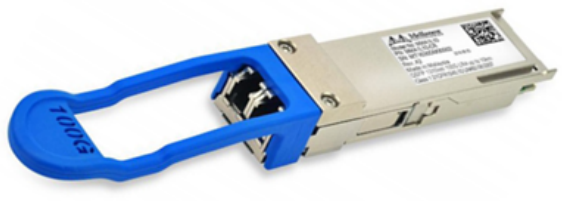
NVIDIA® MMA1L10-CR is a 4-channel pluggable QSFP28 optical transceiver designed for 100 Gigabit Ethernet (GbE) links with up to 10 km reach on a single mode fiber. It is also qualified for use in InfiniBand EDR end-to-end systems.

This transceiver is compliant with the QSFP28 MSA, IEEE 802.3ba 100GBASE-LR4 and IEEE 802.3bm CAUI-4. Digital diagnostic functions are available via the I2C interface, as specified by the QSFP28 MSA.

The MMA1L10-CR module converts 4 input channels of 25 Gb/s electrical data to 4 channels of LAN WDM optical signals at 4 different wavelengths and multiplexes these signals into a single optical transmit signal. On the receiver side, the module de-multiplexes a 100Gb/s optical LAN WDM input into 4 optical signals and then converts these to 4 electrical differential output signals. This transceiver has selectable retiming as specified in the QSFP28 MSA and can therefore be used in both 40 GbE and 100 GbE applications.

Digital diagnostic monitoring functions for temperature, supply voltage, and optical power are available via the two-wire (I2C) management interface, as specified by the QSFP28 MSA [1].

The optical connector is a duplex LC/UPC (un-angled) connector intended for a pair of single mode fibers.
Rigorous production testing ensures the best out-of-the-box installation experience, performance, and durability.



⚠ Images are for illustration purposes only. Product labels and colors may vary.

Key Features

- Hot pluggable QSFP28 MSA form factor
- Compliant to IEEE 802.3ba 100GBASE-LR4 and IEEE 802.3bm CAUI-4 compliant
- Up to 10km reach on Single Mode Fiber (SMF)
- Single +3.3V supply
- Operating case temperature of 0-70°C
- 4x 25.78Gb/s DFB-based LAN-WDM transmitter
- 4x 25.78Gb/s retimed electrical interface
- QSFP28 Power Class 4 (3.5 W max.)
- Duplex LC/UPC optical I/F
- RoHS compliant
- SFF-8636 compliant DDM functions

Applications

- 100GBASE-LR4 100G Ethernet
- 40GBASE-LR4 40G Ethernet
- Qualified for use in NVIDIA InfiniBand EDR end-to-end systems

Pin Description

QSFP28 Pin Function Description

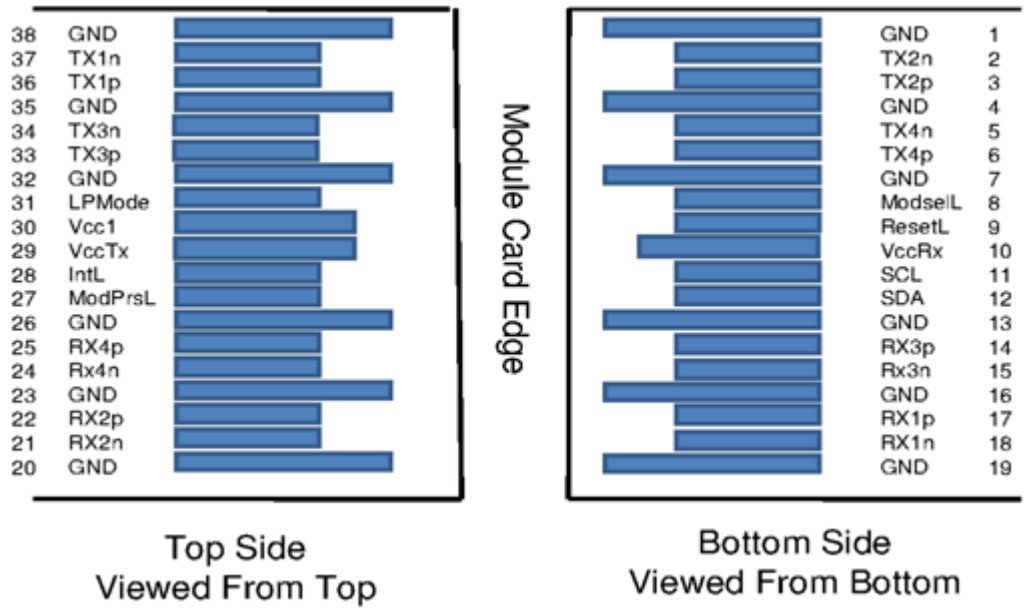
The transceiver's pin assignment is SFF-8679 compliant.

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	20	GND	Ground
2	Tx2n	Transmitter Inverted Data Input	21	Rx2n	Receiver Inverted Data Output
3	Tx2p	Transmitter Non-Inverted Data Input	22	Rx2p	Receiver Non-Inverted Data Output
4	GND	Ground	23	GND	Grounds
5	Tx4n	Transmitter Inverted Data Input	24	Rx4n	Receiver Inverted Data Output
6	Tx4p	Transmitter Non-Inverted Data Input	25	Rx4p	Receiver Non-Inverted Data Output
7	GND	Ground	26	GND	Ground
8	ModSelL	Module Select	27	ModPrsL	Module Present
9	ResetL	Module Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power Supply Receiver	29	Vcc Tx	+3.3V Power Supply Transmitter
11	SCL	2-wire Serial Interface Clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire Serial Interface Data	31	LPMode	Low Power Mode
13	GND	GND	32	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output	33	Tx3p	Transmitter Non-Inverted Data Input
15	Rx3n	Receiver Inverted Data Output	34	Tx3n	Transmitter Inverted Data Input
16	GND	Ground	35	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output	36	Tx1p	Transmitter Non-Inverted Data Input
18	Rx1n	Receiver Inverted Data Output	37	Tx1n	Transmitter Inverted Data Input
19	GND	Ground	38	GND	Ground

Notes:

- GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
- VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently.
- Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000 mA.

QSFP28 Module Pad Layout



Control Signals

This transceiver is SFF-8636 compliant. This means that the control signals shown in the pad layout support the following functions:

Name	Function	Description
ModPrsL	Output, asserted low	Module Present pin, grounded inside the module. Terminated with pull-up in the host system. Asserted low when the transceiver is inserted, whereby the host detects the presence of the transceiver.
ModSelL	Input, asserted Low	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.
ResetL	Input, asserted Low	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. During reset the host shall disregard all status bits until the module indicates completion of the reset interrupt by asserting IntL signal low with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module completes the reset interrupt without requiring a reset.

Name	Function	Description
LPMode	Input, asserted high	Low Power Mode input, pulled up inside the module. The transceiver starts up in low-power mode, i.e. <1.5 W with the two-wire interface active. The host system can read the power class declaration from the transceiver and determine if it has enough power to enable the high-speed operation/ high power mode of the transceiver. This can be done by asserting LPMode low or by use of the Power_over-ride and Power_set control bits (Address A0h, byte 93 bits 0,1).
IntL	Output, asserted low	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’.

The low-speed signals are Low Voltage TTL (LVTTL) compliant (except for SCL and SDA signals).

Diagnostics and Other Features

The transceiver complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis
- Tx/Rx CDR control
  by default enabled for 100 GbE operation, disable it for 40G operation

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the SFF-8636 MSA.

Specifications

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which permanent damage to the device may occur.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-40	85	°C
Operating Case Temperature	T_{OP}	0	70	°C
Maximum Supply Voltage	Vcc	-0.5	3.6	V
Relative Humidity (non-condensing)	RH	15	85	%
Damage Threshold, each Lane	THd	5.5	---	dBm

Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	VccRx, Vcc1, VccTx	3.135	---	3.465	V
Data Rate, each Lane	---	-100 ppm	25.78125	+ 100 ppm	Gbps
Link Distance with G.652 compliant fiber	Lmax	---	---	10	km

Electrical Specifications

Parameter		Symbol	Min	Typical	Max	Units	Notes
Power Consumption		---	---	---	3.5	W	1, 2
Supply Current		Icc	---	---	1.12	A	
Transmitter (each lane)							
Differential Input Voltage Swing		$V_{IN,PP}$	---	---	900	mVpp	
Differential input return loss (min)		RLd(f)	9.5 – 0.37f, 0.01≤f<8 4.75 – 7.4 log10(f/14), 8 ≤f<19			dB	
Differential to common mode input return loss (min)		RLdc(f)	22-20 (f/25.78), 0.01≤f<12.89 15-6 (f/25.78), 12.89≤f<19			dB	
Differential termination mismatch					10	%	
Stressed input parameters							
	Eye width			0.46		UI	
	Applied pk-pk sinusoidal jitter		Per IEEE 802.3bm Table 88-13				

Parameter		Symbol	Min	Typical	Max	Units	Notes
	Eye height			95		mV	
DC common mode voltage			-350	---	2850	mV	
Receiver (each lane)							
Differential Output Voltage Swing		$V_{OUT,PP}$	100	---	400	mVpp	3
			300	---	600		
			400	---	800		
			600	---	1200		
Eye width			0.57	---	---	UI	
Vertical eye closure			---	---	5.5	dB	
Differential output return loss (min)		RLd(f)	9.5 – 0.37f, 0.01≤f<8 4.75 – 7.4log10(f/14), 8 ≤f<19			dB	
Common to differential mode conversion return loss (min)		RLdc(f)	22-20(f/25.78), 0.01≤f<12.89 15-6(f/25.78), 12.89≤f<19			dB	
Differential termination mismatch			---	---	10	%	
Transition time, 20% to 80%		t_r t_f	12	---	---	ps	

Notes:

1. Maximum total power value is specified across the full temperature and voltage ranges.
2. Maximum power consumption for rev. A1 is 4.5 W. Starting from rev. A2 the maximum power consumption is 3.5 W.
3. Output voltage is settable in 4 discrete ranges via I2C. Default range is 400 – 800 mV.

Optical Specifications

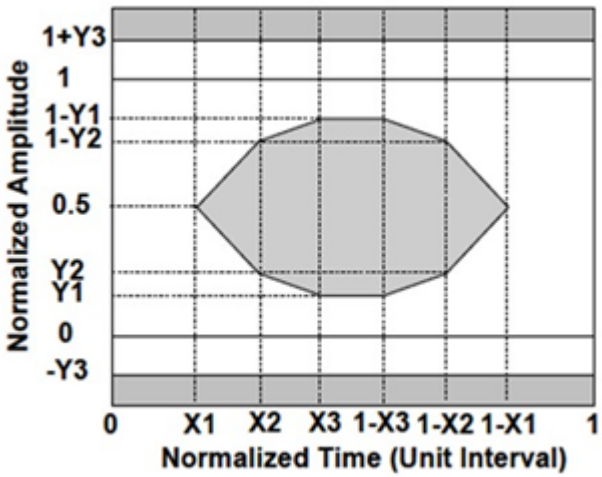
Parameter	Symbol	Min	Typical	Max	Units	Notes
Signaling Speed per Lane		25.78125 ± 100 ppm			Gb/s	1
Lane Wavelength	L0	1294.53	---	1296.59	nm	
	L1	1299.02	---	1301.09	nm	
	L2	1303.54	---	1305.63	nm	
	L3	1308.09	---	1310.19	nm	
Transmitter						
Sidemode Suppression Ratio (SMSR)	SMSR	30	---	---	dB	
Total Average Launch Power	PT	---	---	10.5	dBm	
Average Launch Power, each Lane	P_{AVG}	-4.3		4.5	dBm	2, 7
Optical Modulation Amplitude (OMA), each Lane	P_{OMA}	-1.3	---	4.5	dBm	
Extinction Ratio	ER	4	---	---	dB	
Relative Intensity Noise (RIN)	RIN	---	---	-130	dB/Hz	

Parameter	Symbol	Min	Typical	Max	Units	Notes
Optical Return Loss Tolerance	ORLT	---	---	20	dB	
Transmitter Reflectance	RT	---	---	-12	dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				3
Average Launch Power OFF Transmitter, each Lane	P_{OFF}	---	---	-30	dBm	
Receiver						
Signaling Speed per Lane		25.78125 ± 100 ppm			GBd	4
Receive Power (OMA), each Lane	---	---	---	4.5	dBm	
Average Receive Power per Lane	RXPx	-10.6	---	4.5	dBm	5, 7
Receiver Sensitivity (OMA), each Lane	SEN	---	---	-8.6	dBm	
Stressed Receiver Sensitivity (OMA), each Lane		---	---	-6.8	dBm	6
LOS De-Assert	LOS_D	---	---	-11.6	dBm	
LOS Assert	LOS_A	---	---	-13.6	dBm	
LOS Hysteresis	LOS_H	---	1.5	---	dBm	

Notes:

1. Transmitter consists of 4 lasers operating at 25.78Gb/s each.
2. Minimum value is informative.
3. Hit ratio $5x10^{-5}$.
4. Minimum value is informative, equals min Tx OMA with infinite ER and max channel insertion loss.
5. SRS is measured with vertical eye closure penalty of 1.8 dB max, J2 of 0.30 UI, and J9 of 0.47 UI.
6. Power value and power accuracy are with all channels enabled.

Eye Mask Definition



Electrostatic Discharge (ESD)

This product is compatible with ESD levels in typical data center operating environments and certified in accordance with the standards listed in the Regulatory Compliance Section. The product is shipped with protective caps on all connectors to protect it during shipping. In normal handling and operation of high-speed cables and optical transceivers, ESD is of concern during insertion into the OSFP cage of the server/switch. Hence, standard ESD handling precautions must be observed. These include use of grounded wrist/shoe straps and ESD floor wherever a cable/transceiver is extracted/inserted. Electrostatic discharges to the exterior of the host equipment chassis after installation are subject to system level ESD requirements.

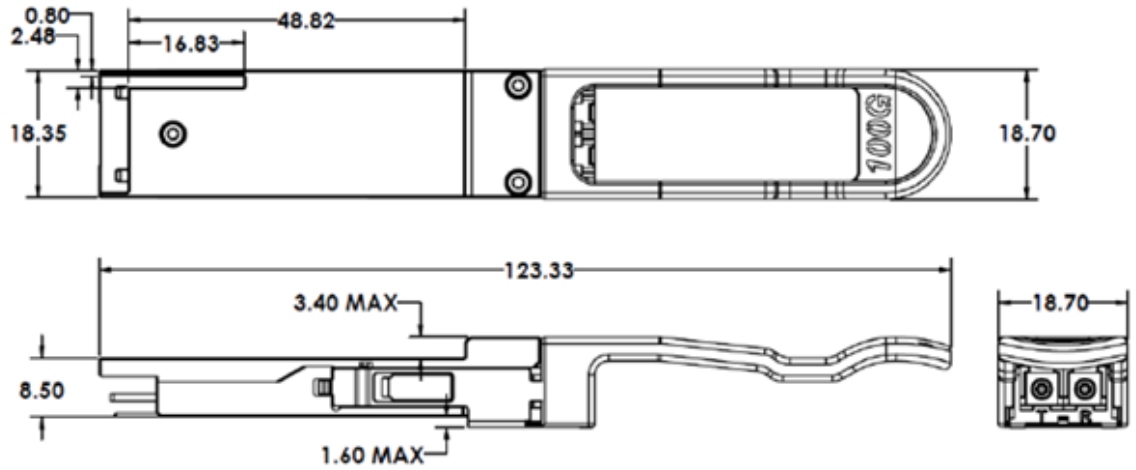
Handling and Cleaning

The transceiver can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Observe normal handling precautions for electrostatic discharge-sensitive devices. The transceiver is shipped with dust caps on both the electrical and the optical port. The cap on the optical port should always be in place when there is no fiber cable connected. The optical connector has a recessed connector surface which is exposed whenever it has no cable nor cap.

Prior to insertion of the fiber cable, clean the cable connector to prevent contamination from it. The dust cap ensures that the optics remain clean and no additional cleaning should be needed. In the event of contamination, standard cleaning tools and methods should be used. Liquids must not be applied.

Mechanical Specifications

Mechanical Dimensions



Memory Map

The transceiver's memory map is compliant with the QSFP Management interface specification SFF-8636. See also the NVIDIA LinkX® Memory Map Application Note (MLNX-15-5926).

Label

The following label is applied on the transceiver's backshell:

(sample illustration)

Backshell Label Legend

Symbol	Meaning	Notes
SN - Serial Number		
MT	Manufacturer name	2 characters (MT)
YY	Year of manufacturing	2 digits
WW	Week of manufacturing	2 digits
DM	Manufacturer site	2 characters
ZZZZZ	Serial number	5 digits for serial number, starting from 00001. Reset at start of week to 00001.
Miscellaneous		

Symbol	Meaning	Notes
ZZ	HW and SW revision	2 alpha-numeric characters
YYYY	Year of manufacturing	4 digits
MM	Month of manufacturing	2 digits
DD	Day of manufacturing	2 digits
COO	Country of origin	E.g. China or Malaysia
	Quick response code	Serial number (MTYYWWXXSSSSS)

Regulatory Compliance and Classification

The laser module is classified as class I according to IEC 60825-1, IEC 60825-2 and 21 CFR 1040 (CDRH).

- Safety: FDA/CDRH, TUV, UL/CSA, ACMA
- EMC: NTS

Ask your NVIDIA FAE for a zip file of the certifications for this product.

FCC Class A Notice

Each of the devices complies with CFR47 FCC Class A Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur during installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

Modifications: Any modifications made to this device that are not approved by NVIDIA may void the authority granted to the user by the FCC to operate this equipment.

Ordering Information

Ordering Part Number	Description
MMA1L10-CR	Optical transceiver, 100GbE, 100Gb/s, QSFP28, LC-LC, 1310nm, LR4 up to 10km

References

1. SFF-8665: “QSFP+ 28Gb/s 4X Pluggable Transceiver Solution (QSFP28)”, and associated SFF documents) available at http://www.snia.org/sff/specifications.
    a. SFF-8661
    b. SFF-8679
    c. SFF-8636
    d. SFF-8662
    e. SFF-8663
    f. SFF-8672
    g. SFF-8683
2. IEEE 802.3ba, PMD Type 100GBASE-LR4.
3. IEEE 802.3bm, Annex 83E, CAUI-4 Interface.
4. Cable and Transceiver Handling and FAQ - NVIDIA Application Note (MLNX-15-3603)
5. Measuring Eye Parameters - NVIDIA Application Note (MLNX-15-5400)

For further information, please contact your sales representative or the NVIDIA support team.

Appendix: Optical Connector and Patch Cable

The optical port in the MMA1L10-CR 100GBASE-LR4 optical transceiver is a duplex LC receptacle.

The cable to use between transceivers of this type is a two-fiber single-mode cable, terminated in duplex LC connectors.

Two fiber single mode cable with duplex LC connectors

One fiber for transmitting, the other for receiving.

Appendix: 40G Operation

This transceiver is SFF-8636 compliant. Its EEPROM contains advertisement bytes (bytes 193, 194 and 224) which contains information on its implemented features. These are read-only and cannot be changed by the host system.

The command registers are used to set programmable functions, i.e. they are writeable, but fall back to their default values when the transceiver is turned off/on. The command registers are bytes 98, 234-239 and have the functions listed below.

The transceiver comprises programmable input equalization in the transmit direction (to the fiber) as well as programmable equalization in the receive direction (from the fiber). Selectable retiming is implemented in all lanes in both transmit and receive direction and is enabled for 100G transmission by default.

Control of Equalizer, Emphasis and Retiming

Page 00 Byte	Bit	Description	Default
193 Advertisement	2	Programmable Tx input equalizers implemented (1 = implemented)	1
	1	Programmable Rx output emphasis implemented (1 = implemented)	1
	0	Programmable Rx output Amplitude (1=implemented)	1
194 Advertisement	7	Tx CDR on/off control implemented (1 = implemented)	1
	6	Rx CDR on/off control implemented (1 = implemented)	1
	5	Tx CDR Loss-of-Lock (LOL) flag implemented (1 = implemented)	1
	4	Rx CDR Loss-of-Lock (LOL) flag implemented (1 = implemented)	1
98 Retiming Control	7	Tx4 CDR control (1 = enabled)	1
	6	Tx3 CDR control (1 = enabled)	1
	5	Tx2 CDR control (1 = enabled)	1
	4	Tx1 CDR control (1 = enabled)	1
	3	Rx4 CDR control (1 = enabled)	1
	2	Rx3 CDR control (1 = enabled)	1
	1	Rx2 CDR control (1 = enabled)	1
	0	Rx1 CDR control (1 = enabled)	1

Note: Set all CDR controls to 0 for 4 x 10 = 40 Gbps operation.

Page 03 Byte	Bit	Description	Default
224 Advertisement	7-4	Maximum Tx input equalization implemented	7
	3-0	Maximum Rx output emphasis implemented	7
234 Control	7-4	Tx1 input Equalizer Control	4
	3-0	Tx2 input Equalizer Control	4
235 Control	7-4	Tx3 input Equalizer Control	4
	3-0	Tx4 input Equalizer Control	4

Page 03 Byte	Bit	Description	Default
236 Control	7-4	Rx1 output Emphasis Control	2
	3-0	Rx2 output Emphasis Control	2
237 Control	7-4	Rx3 output Emphasis Control	2
	3-0	Rx4 output Emphasis Control	2
238 Control	7-4	Rx1 output Amplitude Control	7
	3-0	Rx2 output Amplitude Control	7
239 Control	7-4	Rx3 output Amplitude Control	7
	3-0	Rx4 output Amplitude Control	7

Note: Addresses are in decimal in accordance with the terminology used in SFF-8636.

NVIDIA switches and NICs automatically set both emphasis, amplitude, equalization, and retiming as part of the link-up procedure.

The transceiver's compliance with the SFF-8636 standard allows it to be used in other systems, but the retiming may need to be configured manually and equalization and emphasis may need further optimization for best performance.

Document Revision History

Version	Date	Description of Change
1.6	Nov. 2021	Reformatted and rebranded; migrated to HTML.
1.5	Mar. 2021	Updated the product label. Added Configuration for 40G Operation. Updated document template.
1.4	Sep. 2020	Added 40GbE support information, Control Signals description, optical connector interface + cable specification in Appendix A, and References. Updated DDM info under Diagnostics and Other Features and the Regulatory Compliance and Classification list. Minor text edits.
1.3	Jun. 2018	Introduction and Key Features – Added text about IB support.
1.2	July 19, 2017	New document format. Figure 1– Removed option 1. Table 5: Electrical Module Specifications – Changed Power Consumption from 4.5 to 3.5W, and more. Table 6: Transceiver Optical Specifications – Updated. Regulatory Compliance - New. Removed “Figure: Mechanical Dimensions Option 1”.
1.1	Jan. 19, 2017	Table: Absolute Maximum Ratings: Updated Power Supply Voltage symbols. Table: Recommended Operating Conditions and Power Supply Requirements Updated Power and Voltage symbols, Data Rate min and max values. Table: Electrical Module Specifications– Updated symbols, and Note 1. Table: Transceiver Optical Specifications Updated symbols and notes Table: Back-Shell Label Legend - New. Appendix: Parallel Fiber Cables for 4 Channel Transceivers – Removed.
1.0	Dec. 20, 2016	Initial release.

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