

# MMA1T00-HS HDR QSFP56 MMF Transceiver Product Specifications

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## Introduction

The NVIDIA<sup>®</sup> MMA1T00 transceiver is a 4channel, pluggable, QSFP56 optical transceiver, designed for use in 200Gb/s HDR InfiniBand applications. This module incorporates NVIDIA integrated circuit technology, in order to provide high performance. The transceiver operates over 4-lane parallel multi-mode fiber (MMF), using a nominal wavelength of 850nm, and is QSFP56 MSA compliant.

The transceiver has a standard SFF-8665 compliant QSFP56 connector on the electrical side towards the host system. The optical interface is composed of four optical channels/ fibers in each direction, intended for a parallel multi-mode optical cable via a standard MPO-12 UPC connector. Each channel/fiber operates at signaling rates up to 26.5625 GBd. Rigorous production testing ensures the best out-of-thebox installation experience, performance and durability.

The MMA1T00 transceiver has Digital Diagnostic Monitoring (DDM) functions for supply voltage, temperature, laser bias current, optical transmit and receive levels with associated warning and alarm thresholds.

The MMA1T00 transceiver will work with a fiber plant as specified in the QSFP MSA standard.



Images are for illustration purposes only. Product labels and colors may vary.

#### **Key Features**

- Up to 200Gb/s
- Up to 100m on OM4 and 70m on OM3 multimode fiber at 200Gb/s
- 4 x 50Gb/s PAM4 modulation
- Programmable Rx output amplitude and emphasis
- Adaptive Tx input equalizer
- SFF-8665 compliant QSFP56 port
- SFF-8636 DDM compliant
- Single 3.3V power supply
- 4.35W typ power consumption
- QSFP56 power class 7
- Class 1 laser safety
- Hot pluggable
- RoHS compliant
- MPO-12 UPC male receptacle connector
- SFF-8636 compliant I<sup>2</sup>C management interface

#### **Applications**

• InfiniBand HDR and EDR links

## Pin Description

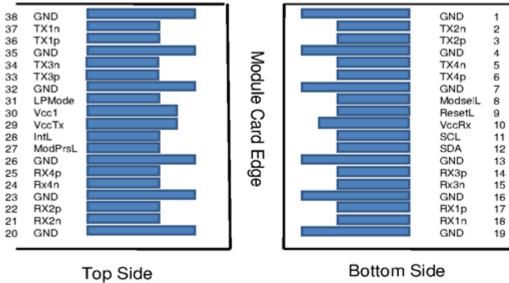
The MMA1T00 transceiver is compliant with the MSA Specification for Quad Small Form Factor Pluggable (QSFP) Transceiver specification, see [1] and [2].

The transceiver's pin assignment is SFF-8679 compliant [3].

#### **QSFP56** Pin Function Definition

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	20	GND	Ground
2	Tx2n	Transmitter Inverted Data Input	21	Rx2n	Receiver Inverted Data Output
3	Tx2p	Transmitter Non-Inverted Data Input	22	Rx2p	Receiver Non-Inverted Data Output
4	GND	Ground	23	GND	Grounds
5	Tx4n	Transmitter Inverted Data Input	24	Rx4n	Receiver Inverted Data Output
6	Tx4p	Transmitter Non-Inverted Data Input	25	Rx4p	Receiver Non-Inverted Data Output
7	GND	Ground	26	GND	Ground
8	ModSelL	Module Select	27	ModPrsL	Module Present
9	ResetL	Module Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power Supply Receiver	29	Vcc Tx	+3.3V Power Supply Transmitter
11	SCL	2-wire Serial Interface Clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire Serial Interface Data	31	LPMode	Low Power Mode
13	GND	GND	32	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output	33	Тх3р	Transmitter Non-Inverted Data Input
15	Rx3n	Receiver Inverted Data Output	34	Tx3n	Transmitter Inverted Data Input
16	GND	Ground	35	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output	36	Tx1p	Transmitter Non-Inverted Data Input
18	Rx1n	Receiver Inverted Data Output	37	Tx1n	Transmitter Inverted Data Input
19	GND	Ground	38	GND	Ground

#### **QSFP56 Module Pad Layout**



Viewed From Top

Viewed From Bottom

#### **Control Signals**

The MMA1T00 transceiver is SFF-8636 compliant. This means that the control signals shown in the pad layout support the following functions:

ModPrsL	Module Present pin, grounded inside the module. Terminated with pull-up in the host system. Asserted low when the transceiver is inserted, whereby the host detects the presence of the transceiver.
ModSelL	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.
ResetL	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. During reset the host shall disregard all status bits until the module indicates completion of the reset interrupt by asserting IntL signal low with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module completes the reset interrupt without requiring a reset.
LPMode	Low Power Mode input, pulled up inside the module. The transceiver starts up in low power mode, i.e. <1.5 W with the two-wire interface active. The host system can read the power class declaration from the transceiver and determine if it has enough power to enable the high-speed operation/high power mode of the transceiver. This can be done by asserting LPMode low or by use of the Power_over- ride and Power_set control bits (Address A0h, byte 93 bits 0,1).
IntL	Interrupt Low is an open-collector output, terminated high in the host system. A "Low" indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface. The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0'.

The low-speed signals are Low Voltage TTL (LVTTL) compliant, except for SCL and SDA signals.

## Handling and Cleaning Precautions

The transceiver can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Observe normal handling precautions for electrostatic discharge-sensitive devices. The transceiver is shipped with dust caps on both the electrical and the optical port. The cap on the optical port should always be in place when there is no fiber cable connected. The optical connector has a recessed connector surface which is exposed whenever it has no cable nor cap.

Prior to insertion of the fiber cable, clean the cable connector to prevent contamination from it. The dust cap ensures that the optics remain clean and no additional cleaning should be needed. In the event of contamination, standard cleaning tools and methods should be used. Liquids must not be applied.

# Specifications

## Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Parameter	Min	Max	Units
Supply voltage	-0.3	3.6	V
Data input voltage	-0.3	3.465	V
Control input voltage	-0.3	4.0	V
Damage threshold	3.4		dBm

## **Environmental Specifications**

This table shows the environmental specifications for the product.

Parameter	Min	Max	Units
Storage temperature	-40	85	°C

## **Operational Specifications**

This section shows the range of values for normal operation.

Parameter	Min	Тур	Max	Units
Supply voltage (V <sub>cc</sub> )	3.135	3.3	3.465	V
Power consumption (each end, retiming on all lanes)		4.35	5.0	W
Supply noise tolerance (10Hz - 10MHz)	66			mVpp
Operating case temperature	0		70	°C
Operating relative humidity	5		85	%

## **Electrical Specifications**

Parameter (per lane)	Min	Тур	Max	Units
Signaling rate	-100 ppm	26.5625	+100 ppm	GBd
Differential data input swing at TP1a			900	mVpp
Differential data output swing at TP4			900	mVpp

Parameter (per lane)	Min	Тур	Max	Units
Near-end ESMW (Eye Symmetry Mask Width)	0.265			UI
Near-end output eye height	70			mVpp
Output transition time, 20% to 80%	9.5			ps

Notes:

- Multiple clock domains are supported only on line-side Rx. Host side Rx supports a single clock domain only.
- QSFP Tx CDR lock can only occur if Tx lane 1 is transmitting data.

## **Optical Specifications**

Parameter	Min	Тур	Max	Units		
Transmitter (per lane)						
Signaling speed (with retiming)	-100 ppm	26.5625	+100 ppm	GBd		
Center wavelength	840	850	860	nm		
Spectral width			0.6	nm		
Average launch power	-2.0		3.0	dBm		
Transmit OMA	-2.0		3.0	dBm		
Average launch power of off transmitter			-30	dBm		
Extinction ratio	4.0		6.0	dB		
Transmitter reflectance tolerance			-12.0	dB		
Transmitter return loss			-18.0	dB		
Transmitter eye mask definition						
Reach on OM3 multi-mode fiber	100			m		
Receiver (per lane)	<u>.</u>			·		
Signaling speed (with retiming)	-100 ppm	26.5625	+100 ppm	GBd		
Center wavelength	840	850	860	nm		
Receive damage threshold (AOP)	5.0			dBm		
Unstressed receiver sensitivity (OMA) at BER = $10^{-6}$			-5.0	dBm		
Receiver Reflectance			-18.0	dB		
LOS assert			-14	dBm		
LOS hysteresis	0.5		3.0	dB		
Stressed receiver sensitivity (OMA) at BER = 10 <sup>-4</sup>			-3.0	dBm		
Conditions of stressed receiver sensiti	Conditions of stressed receiver sensitivity test					
SECQ (Stressed Eye Closure) penalty			4.9	dB		
OMA of each aggressor lane			3.0	dB		
Stressed eye mask definition	TBD					

The receiver's performance may degrade due to overload if the maximum values for AOP or OMA are exceeded. The damage threshold is specified in the <u>Absolute Maximum Ratings</u> table above.

## **Rate Select**

The MMA1T00 transceiver supports rate select, which is controlled by writing to registers 0x57-0x58. Two bits are assigned for each receiver lane in byte 0x57 (87dec, Rxn\_Rate\_Select) and two bits for each transmitter lane in byte 0x58 (88dec, Txn\_Rate\_Select) to specify up to four bitrates, as defined in SFF-8636 Rev 2.9.2 Table 6-5 XN\_RATE\_SELECT ENCODINGS. All four lanes are required to have the same rate select value.

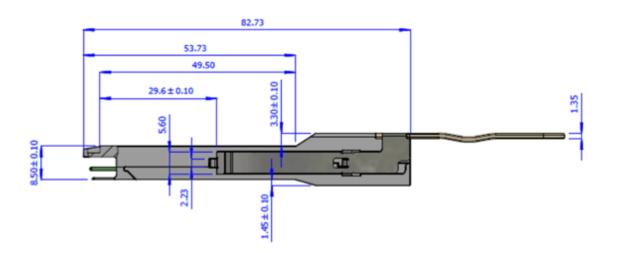
The below table specifies the rate for each rate select setting.

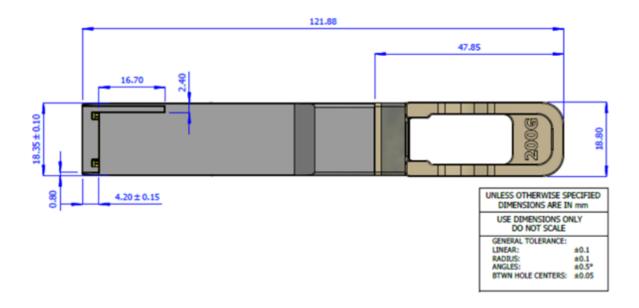
#### Rate Select Encodings

Rate Select Value	Operating Rate (GBd)
01	10.31250 NRZ
10	25.78125 NRZ
11	26.56250 PAM4

## **Mechanical Specifications**

#### **Mechanical Dimensions**





#### Label Description

The following label is applied on the transceiver's backshell:

#### Backshell Label

Model No: MMA1T00 PN: MMA1T00-HS SN: MTYYWWXXSSSSS Rev: ZZ YYYY-MM-DD Made In COO		
QSFP56 850nm 200G up to 100m Class 1 21CFR1040.10 LN#56 05/2019 Mellanox		

(sample illustration)

### Backshell Label Legend

Symbol	Meaning	Notes			
SN - Serial Number	SN - Serial Number				
мт	Manufacturer name	2 characters, e.g. MT			
YY	Year of manufacturing	2 digits			
WW	Week of manufacturing	2 digits			
FT	Manufacturer site	2 characters			
ZZZZZ	Serial number	5 digits for serial number, starting from 00001. Reset at start of week to 00001.			
Miscellaneous	·	·			
ZZ	HW and SW revision	2 alpha-numeric characters			
YYYY	Year of manufacturing	4 digits			
MM	Month of manufacturing	2 digits			
DD	Day of manufacturing	2 digits			
C00	Country of origin	E.g. Thailand			
	Quick response code	Serial number (MTYYWWFTZZZZZ)			

#### Regulatory Compliance and Classification Transceiver

The laser module is classified as Class 1 according to IEC 60825-1, IEC 60825-2 and 21 CFR sub J 1040 (CDRH), TÜV/UL60950-1, CAN/CSA-C22.2 60950-1.

EMC: EN55032 Class A, EN55024, AS/NZS CISPR 32 Class A, CISPR32 Class A, VCCI Class A.

Telcordia Technologies© GR-468CORE, (shock, vibration, HT operation, damp heat operation).

Ask your NVIDIA field engineer or the support team for a zip file of the certifications for this product.

## FCC Class A Notice

This device complies with CFR47 FCC Class A Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- 1. This device may not cause harmful interference.
- 2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

Modifications: Any modifications made to this device that are not approved by NVIDIA may void the authority granted to the user by the FCC to operate this equipment.



# Ordering Information

Ordering Part Number	Description
MMA1T00-HS	Transceiver, HDR, QSFP56, MPO, 850nm, SR4, up to 100m

## References

- 1. QSFP Quad Small Form Factor Pluggable Concept: SFF-8665: https://www.snia.org/technology-communities/sff/specifications
- 2. QSFP Quad Small Form Factor Pluggable Management: SFF-8636: <u>https://www.snia.org/technology-communities/sff/specifications</u>
- 3. QSFP Quad Small Form Factor Pluggable Hardelectrical: SFF-8679: https://www.snia.org/technology-communities/sff/specifications
- InfiniBand Architecture Specification and FAQ: <u>https://www.infinibandta.org/ibta-specification/</u>
- 5. Environmental and Regulatory compliance statements: <u>https://www.mellanox.com/company/quality/regulatory-compliance/environmental</u>
- 6. Nvidia Networking Cable Configurator: <u>https://www.mellanox.com/products/interconnect/cables-configurator</u>
- 7. LinkX\_MemoryMap\_Application\_Note (MLNX-15-5926)
- 8. Measuring\_Eye\_Parameters\_100GbE\_Modules\_Application\_Note (MLNX-15-5400)
- 9. NVIDIA\_Cable\_Management\_Guidelines\_and\_FAQs\_Application\_Note (MLNX-15-3603)

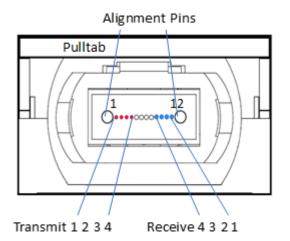
For documentation, please contact your sales representative or the Support team.

## Appendix: Optical Connector and Fiber Cable

## **Optical Connector**

The optical port in the parallel  $2 \times 4$ -lane optical transceiver is a male MPO connector with alignment pins, mating with fiber-optic cables with female MPO connector.

# QSFP28 Optical Receptacle and Lane Assignment (transceiver, front view)



Reference: IEC specification IEC 61754-7.

#### Fiber Patch Cable

The fiber which connects transceiver A's lane 1 must end at transceiver B's lane 12 at the other end of the link. This calls for a crossed MPO cable, also referred to as 'Type B'. The fiber is standard OM3 or OM4 multi-mode fiber. The maximum length is found in <u>Optical Specifications</u>.

#### MPO to MPO Patch Cable Fiber Connections

Connector A MPO/UPC Female	Connection	Connector B MPO/UPC Female
1	$\rightarrow$	12
2	$\rightarrow$	11
3	$\rightarrow$	10
4	$\rightarrow$	9
5	Not Connected	8
6	Not Connected	7

Connector A MPO/UPC Female	Connection	Connector B MPO/UPC Female
7	Not Connected	6
8	Not Connected	5
9	←	4
10	←	3
11	←	2
12	←	1

Multiple MPO patch cables can be connected in series, but each added connector pair increases modal dispersion in the link which again impairs performance. An odd number of 'crosses' must be used between transceivers at the two ends.

#### Typical look of the Fiber Cable





OM3 Multimode Cable Some vendors use aqua color for OM4 cables. OM4 Multimode Cable

# Document Revision History

Revision	Date	Description
1.4	Nov. 2021	Reformatted and rebranded; migrated to HTML. Removed BER bullet.
1.3	Feb. 2021	Updated Key Features section. Removed 2.5G/SDR from Table: Rate Select Encodings. Minor text edits.
1.2	Nov. 2020	Added Applications, control signal description, Handling and cleaning precautions, and references. Updated patch cable specification.
1.1	Nov. 2019	Changed "Key Features" item on MPO-12 UPC to indicate male receptacle connector
1.0	Sep. 2019	Initial release

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