MMS1V70-CM 100GbE QSFP28 DR1 Transceiver Product Specifications

Exported on Jan/02/2024 05:56 PM

Table of Contents

Introduction

NVIDIA® MMS1V70-CM transceiver is a single mode 1-lane (DR1), QSFP28 optical transceiver, designed for use in 100 Gigabit Ethernet (GbE) links on up to 500m of single mode fiber.

The transceiver converts 4 input channels of 25Gb/s NRZ electrical data to a single optical channel of 100Gb/s PAM4 optical signals over a single fiber, using a nominal wavelength of 1310nm, and vice versa for the receive path. The MMS1V70-CM main application is to converge between legacy 100GbE NRZ systems and the emerging 400GbE PAM4 systems. Four different MMS1V70-CM transceivers can be connected to a single 400GbE QSFP-DD MMS1V00-WM DR4 transceiver over a single mode splitter cable.

It is compliant with the QSFP28 MSA, IEEE 802.3bm CAUI-4. Digital diagnostic functions are available via the I2C interface, as specified by the QSFP28 MSA.

Rigorous production testing ensures the best out-of-the-box installation experience, performance, and durability.

Images are for illustration purposes only. Product labels and colors may vary.

Key Features

- 4x 25Gb/s NRZ Modulation
- Programmable Rx output amplitude and pre-emphasis
- SFF-8665 compliant QSFP56 port
- Single 3.3V power supply
- 4W max power dissipation (typ., each end, with retiming)
- Up to 500m length
- Hot pluggable
- RoHS compliant
- SFF-8636 compliant I2C management interface

Applications

- Supports 4x MMS1V70-CM on MSN2700 to a single MMS1V00-WM on MSN4700

Pin Description

The transceiver's pin assignment is SFF-8679 compliant.

Table 2: QSFP28 Pin Function Definition

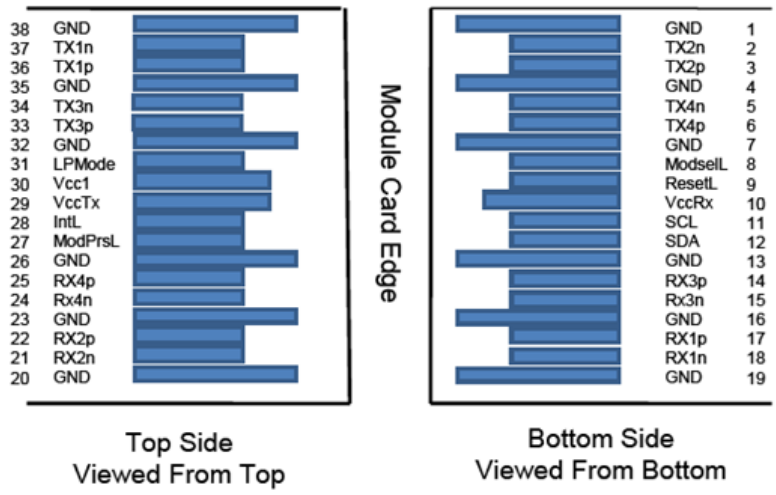
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModselL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	

Pin	Logic	Symbol	Description	Plug Sequence	Notes
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering see SFF-8679.

QSFP28 Module Pad Layout:



Control Signals

The MMS1V70 is SFF-8636 compliant, thus the control signals shown in the pad layout are implemented with the following functions:

ModPrsL	Output, asserted low	Pull-up by host when no transceiver/cable is present. Connected to ground inside the transceiver. Hence, asserted low when a transceiver/cable is plugged in.
ModSelL	Input, asserted Low	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.
ResetL	Input, asserted Low	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum length initiates a module reset. When de-asserted the transceiver starts its initialization procedure. See the CMIS specification **Error! Reference source not found.** for details.
LPMode	Input, asserted high	Low Power Mode input, pulled up inside the module. Hardware control signal for forcing the transceiver into low-power state. Can be overwritten by low-power mode command.
IntL	Output, asserted low	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface.

The low-speed signals are Low Voltage TTL (LVTTL) compliant (except for SCL and SDA signals).

Diagnostics and Other Features

The transceiver complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis
- Tx/Rx CDR control
  by default enabled for 100 GbE operation, disable it for 40G operation

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the SFF-8636 MSA.

Specifications

Absolute Maximum Specifications

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module

Parameter	Symbol	Min	Max	Units
Storage Temperature	TS	-40	+85	℃
Supply Voltage	VCC	-0.3	3.6	V
Relative Humidity (non-condensing)	RH	5	95	%
Data Input Voltage – Differential	lVDIP-VDINl	-	1.0	V
Control Input Voltage	VI	-0.3	Vcc+0.5	V
Control Output Current	IO	-20	20	mA

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0	-	70	℃	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP	-	-	1600	mA	
Sustained peak current at hot plug	ICC_SP	-	-	1320	mA	
Maximum Power Dissipation	PD	-	-	4	W	1
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	1.5	W	
Signalling Rate	SR	-	53.125	-	GBd	
Control Input Voltage High	V_{IH}	V_{CC}*0.7	-	V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3	-	V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise	-	-	-	66	mVpp	10Hz -10MHz
Rx Differential Data Output Load	-	-	100	-	ohms	
Operating Distance	-	2	-	500	m	

Note 1: with power supply voltage 3.3V.

Optical Specifications

Parameter	Symbol	Min.	Typical	Max.
Transmitter				
Wavelength	λ_C	1304.5	1311	1317.5
Side mode suppression ratio	SMSR	30	-	-
Average Optical Launch Power	P_{OUT}	-2.9	-	4
Average Launch Power Tx_Off	P_{OUT_OFF}	-	-	-15
Extinction Ratio	ER	3.5	-	-
Outer Optical Modulation Amplitude	OMA_{outer}	-0.8	-	4.2
Launch Power in OMA_{outer} minus TDECQ for ER ≥ 5dB	OMA_{outer}-TDECQ	-2.2	-	-
Launch Power in OMA_{outer} minus TDECQ for ER < 5dB	OMA_{outer}-TDECQ	-1.9	-	-
Transmitter and dispersion eye closure	TDECQ	-	-	3.4
TDECQ-$10\log_{10}(C_{eq})$		-	-	3.4
Transmitter transition time	T_{Tx}	-	-	17
$RIN_{15.5}OMA$	RIN	-	-	-136
Optical return loss tolerance	ORLT	-	-	15.5
Transmitter reflectance	TR	-	-	-26
Receiver				
Wavelength	λ_C	1304.5	1311	1317.5
Damage Threshold		5	-	-
Average receive power		-5.9	-	4
Receive power (OMA_{outer})	RP	-	-	4.2
Receiver reflectance	RR	-	-	-26
Receiver sensitivity (OMA_{outer})	RS	max(-3.9, SECQ-5.3)	dBm	
Stressed receiver sensitivity	SRS	-	-	-1.9
Stressed Receiver Sensitivity Test Conditions:				
Stressed eye closure for PAM4 (SECQ)	SECQ	-	-	3.4
SECQ-$10\log_{10}(C_{eq})$	-	-	-	3.4

Note: Amplitude customization beyond these specs is dependent on validation in customer system.

Electrical Specifications

Low-Speed Signal: Compliant to SFF-8679

High-Speed Signal: Compliant to CAUI-4 (IEEE 802.3-2018)

Support for 100GAUI-4 at 26.5625 Gbd when using KP4 FEC

Parameter	Symbol	Min.	Typical	Max.	Unit	No
Transmitter						
LPMode, Reset and ModSelL	V_{IL}	-0.3	-	Vcc*0.3	V	
	V_{IH}	V_{CC}*0.7	-	V_{CC}+0.3	V	
Differential Data Input Amplitude	$V_{IN,P-P}$	95	-	900	mVpp	Note 1
Differential Termination Mismatch		-	-	10	%	
Receiver						
ModPrsL and IntL	V_{OL}	0	-	0.4	V	I_{OL}=4m
	V_{OH}	V_{CC}-0.5	-	V_{CC}+0.3	V	I_{OL}=-4m
Differential Data Output Amplitude	$V_{OUT,P-P}$	250	-	900	mVpp	Note 1
Differential Termination Mismatch		-	-	10	%	
Output Rise/Fall Time, 20%~80%	T_R	9.5	-	-	ps	

Note: Amplitude customization beyond these specs is dependent on validation in customer system.

Handling and Cleaning

The transceiver can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Observe normal handling precautions for electrostatic discharge-sensitive devices. The transceiver is shipped with dust caps on both the electrical and the optical port. The cap on the optical port should always be in place when there is no fiber cable connected. The optical connector has a recessed connector surface which is exposed whenever it has no cable nor cap.

Prior to insertion of the fiber cable, clean the cable connector to prevent contamination from it. The dust cap ensures that the optics remain clean and no additional cleaning should be needed. In the event of contamination, standard cleaning tools and methods should be used. Liquids must not be applied.

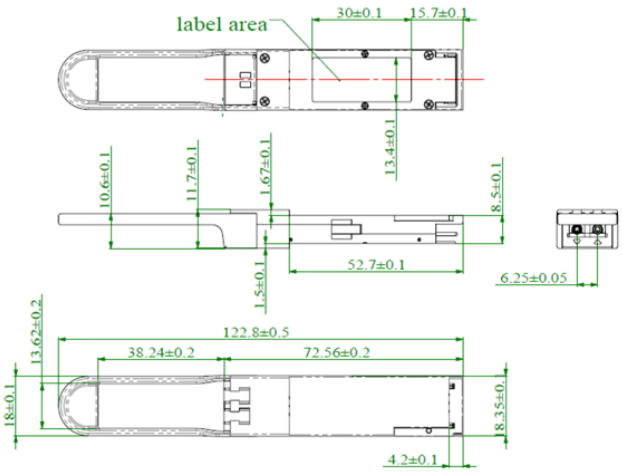
Regulatory Compliance

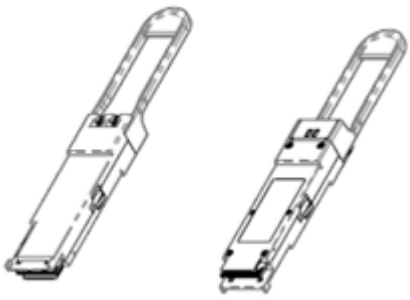
The transceiver is a Class 1 laser product. It is certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50
Electrical Safety	CB	IEC 60950-1
Electrical Safety	UL/CSA	UL 60950-1 and CAN/CSAN 60950-1

Mechanical Specifications

Mechanical Dimensions



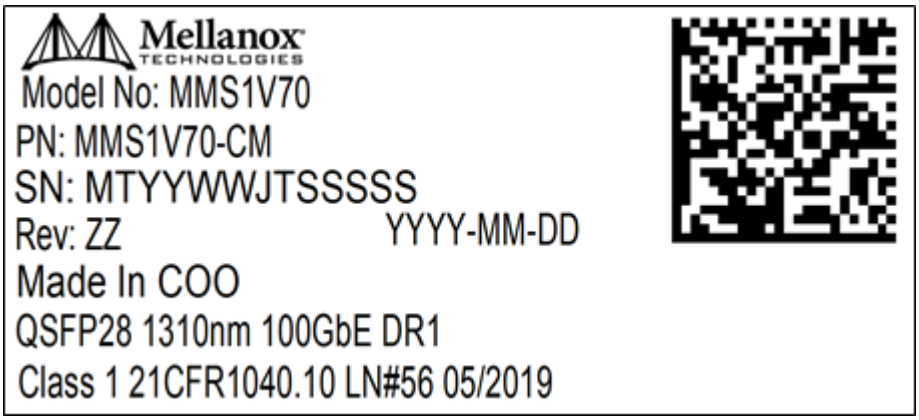


Memory Map

See LinkX® Memory Map Application Note (MLNX-15-5926).

Label

An example of the label applied on the transceiver's back-shell is illustrated below.



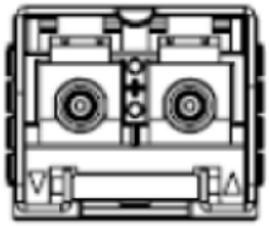
Images are for illustration purposes only. Product labels and colors may vary.

Transceiver Back-Shell Label Serial Number Legend

Symbol	Meaning	Notes
MT	Manufacturer name (Mellanox/NVIDIA)	2 digits (alphanumeric)
YY	Year of manufacturing	2 last digits of the year (numeric)
WW	Week of manufacturing	2 digit (numeric)
JT	Manufacturer Site: JT (Taiwan)	Two characters
SSSSS	Serial number	5 digits (decimal numeric) for serial number, starting from 00001.
MM	Month	2 digit (numeric)
DD	Day	2 digit (numeric)
ZZ	Revision Number	2 digits (alphanumeric)

Appendix A: Optical Connector and Fiber Cable

The optical port in the transceiver is a pair of LC connectors which mate with fiber-optic cables with duplex LC connector.



Optical LC Receptacle (transceiver, front view)

Reference: IEC specification IEC 61754-20.

The fiber which connects transceiver A's lane 1 must end at transceiver B's lane 2 at the other end of the link. This calls for a crossed cable, also referred to as 'Type B'. The fiber is standard single mode fiber.

Table 8: LC to LC Cable Fiber Connections

Connector A Duplex LC	Connection	Connector B Duplex LC
1	--->	2
2	<---	1

Multiple LC patch cables can be connected in series, but each added connector pair adds reflections and modal dispersion in the link which again impairs performance. An odd number of 'crosses' must be used between transceivers at the two ends.

Typical look of a Single Mode LC Fiber Patch Cable:

Remember to clean the connectors with a fiber cleaner before plugging the cable in.

Ordering Information

Part Numbers and Description

OPN	Description
MMS1V70-CM	Mellanox® transceiver, 100GbE, QSFP28, LC-LC, 1310nm, DR1

References

- L QSFP Quad Small Form Factor Pluggable – Concept: SFF-8665: https://www.snia.org/technology-communities/sff/specifications
- QSFP Quad Small Form Factor Pluggable – Management: SFF-8636: https://www.snia.org/technology-communities/sff/specifications
- InfiniBand Architecture Specification and FAQ: https://www.infinibandta.org/ibta-specification/
- Environmental and Regulatory compliance statements: https://www.nvidia.com/en-us/networking/environmental-and-regulatory-compliance/
- NVIDIA Networking Cable Configurator: https://www.nvidia.com/en-us/networking/configuration-tools/

For documentation, please contact your sales representative.

Revision History

Version	Date	Description of Change
1.1	Jan. 2022	Updated Power Dissipation typo in Key Features section.
1.0	Jul. 2021	First release.

Notice

This document is provided for information purposes only and shall not be regarded as a warranty of a certain functionality, condition, or quality of a product. Neither NVIDIA Corporation nor any of its direct or indirect subsidiaries and affiliates (collectively: “NVIDIA”) make any representations or warranties, expressed or implied, as to the accuracy or completeness of the information contained in this document and assumes no responsibility for any errors contained herein. NVIDIA shall have no liability for the consequences or use of such information or for any infringement of patents or other rights of third parties that may result from its use. This document is not a commitment to develop, release, or deliver any Material (defined below), code, or functionality.

NVIDIA reserves the right to make corrections, modifications, enhancements, improvements, and any other changes to this document, at any time without notice. Customer should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

NVIDIA products are sold subject to the NVIDIA standard terms and conditions of sale supplied at the time of order acknowledgement, unless otherwise agreed in an individual sales agreement signed by authorized representatives of NVIDIA and customer (“Terms of Sale”). NVIDIA hereby expressly objects to applying any customer general terms and conditions with regards to the purchase of the NVIDIA product referenced in this document. No contractual obligations are formed either directly or indirectly by this document.

NVIDIA products are not designed, authorized, or warranted to be suitable for use in medical, military, aircraft, space, or life support equipment, nor in applications where failure or malfunction of the NVIDIA product can reasonably be expected to result in personal injury, death, or property or environmental damage. NVIDIA accepts no liability for inclusion and/or use of NVIDIA products in such equipment or applications and therefore such inclusion and/or use is at customer’s own risk.

NVIDIA makes no representation or warranty that products based on this document will be suitable for any specified use. Testing of all parameters of each product is not necessarily performed by NVIDIA. It is customer’s sole responsibility to evaluate and determine the applicability of any information contained in this document, ensure the product is suitable and fit for the application planned by customer, and perform the necessary testing for the application in order to avoid a default of the application or the product. Weaknesses in customer’s product designs may affect the quality and reliability of the NVIDIA product and may result in additional or different conditions and/or requirements beyond those contained in this document. NVIDIA accepts no liability related to any default, damage, costs, or problem which may be based on or attributable to: (i) the use of the NVIDIA product in any manner that is contrary to this document or (ii) customer product designs.

No license, either expressed or implied, is granted under any NVIDIA patent right, copyright, or other NVIDIA intellectual property right under this document. Information published by NVIDIA regarding third-party products or services does not constitute a license from NVIDIA to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property rights of the third party, or a license from NVIDIA under the patents or other intellectual property rights of NVIDIA.

Reproduction of information in this document is permissible only if approved in advance by NVIDIA in writing, reproduced without alteration and in full compliance with all applicable export laws and regulations, and accompanied by all associated conditions, limitations, and notices.

THIS DOCUMENT AND ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, “MATERIALS”) ARE BEING PROVIDED “AS IS.” NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY, OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE. TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL NVIDIA BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF NVIDIA HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Notwithstanding any damages that customer might incur for any reason whatsoever, NVIDIA’s aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms of Sale for the product.

Trademarks

NVIDIA, the NVIDIA logo, and Mellanox are trademarks and/or registered trademarks of NVIDIA Corporation and/or Mellanox Technologies Ltd. in the U.S. and in other countries. Other company and product names may be trademarks of the respective companies with which they are associated.