



**MMS4X90-NR 800Gbps, 2xLR4, OSFP, 2xLC-LC, 1310nm
SMF, Finned Twin-port Transceiver (up to 10km)**

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Introduction

The NVIDIA MMS4X90-NR is an 800Gb/s 2x400Gb/s Twin-port OSFP, 2xLR4 single mode, 8-channel electrical transceiver. This transceiver uses two, 2-fiber, LC Duplex optical connectors each carrying 4-channels of 100G-PAM4. The 8-channel 2xLR4 design uses 100G-PAM4 electrical and optical modulation based on the CWDM4 serial, multiplexed 1310nm wavelength grid.

It has a maximum fiber reach of 2,000-meters which assumes two optical patch panels in the link. The transceiver firmware supports Ethernet.

The Twin-port 2xLR4 transceiver has two internal transceiver engines enabling 128-ports of 400Gb/s Spectrum-4 switches have 64 cages .

The main application for MMS4X90-NR is linking two switches together up to 10,000-meter.

The transceiver combinations guarantee optimal operation in NVIDIA end-to-end InfiniBand systems and a rigorous production tested to ensure the best out-of-the-box installation experience, performance, and durability.



Note

Images are for illustration purposes only. Product labels, colors, and lengths may vary.

Key Features

- 800G 2xLR4 single mode
- 8-channels of 100G-PAM4 electrical modulation
- Two Duplex LC ports of 4-channel 100G-PAM4 optical modulation
- Supports two single mode fiber cables with duplex LC optical connectors
- 8x 1330nm EML lasers
- 10km Max reach
- 17-Watts max power
- Single 3.3V power supply
- Class 1 laser safety
- Hot pluggable, RoHS compliant
- [OSFPmsa.org](https://www.osfpmsa.org) compliant
- CMIS 5.0 compliant

Fibers not supplied by NIVIDIA

Applications

- Used to link Spectrum-4 air-cooled switches together.

Pin Description

The device is OSFP MSA Specification for OSFP Octal Small Form Factor Pluggable Module Rev. 1.12 compliant, see www.osfpmsa.org.

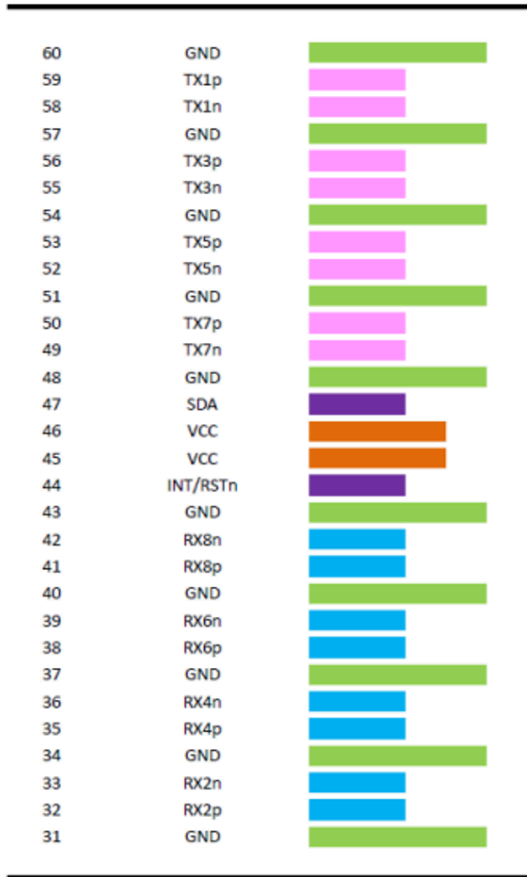
OSFP Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	31	GND	Ground
2	Tx2p	Transmitter Non-Inverted Data Input	32	Rx2p	Receiver Non-Inverted Data Output
3	Tx2n	Transmitter Inverted Data Input	33	Rx2n	Receiver Inverted Data Output
4	GND	Ground	34	GND	Grounds
5	Tx4p	Transmitter Non-Inverted Data Input	35	Rx4p	Receiver Non-Inverted Data Output
6	Tx4n	Transmitter Inverted Data Input	36	Rx4n	Receiver Inverted Data Output
7	GND	Ground	37	GND	Ground
8	Tx6p	Transmitter Non-Inverted Data Input	38	Rx6p	Receiver Non-Inverted Data Output
9	Tx6n	Transmitter Inverted Data Input	39	Rx6n	Receiver Inverted Data Output
10	GND	Ground	40	GND	Ground
11	Tx8p	Transmitter Non-Inverted Data input	41	Rx8p	Receiver Non-Inverted Data Output
12	Tx8n	Transmitter Inverted Data Input	42	Rx8n	Receiver Inverted Data Output
13	GND	Ground	43	GND	Ground
14	SCL	2-wire serial interface clock	44	INT / RSTn	Module Interrupt / Module Reset

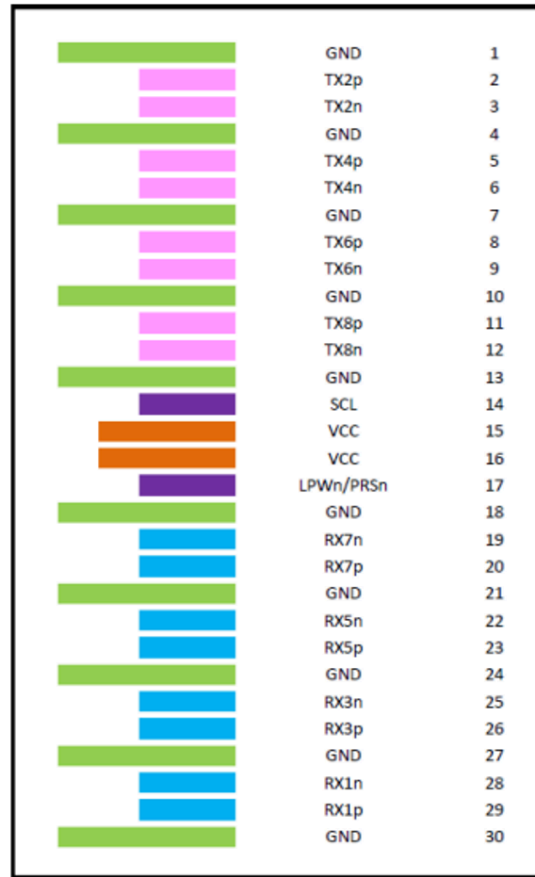
Pin	Symbol	Description	Pin	Symbol	Description
15	VCC	+3.3V Power	45	VCC	+3.3V Power
16	VCC	+3.3V Power	46	VCC	+3.3V Power
17	LPWn / PRSn	Low-Power Mode / Module Present	47	SDA	2-wire Serial interface data
18	GND	Ground	48	GND	Ground
19	Rx7n	Receiver Inverted Data Output	49	Tx7n	Transmitter Inverted Data Input
20	Rx7p	Receiver Non-Inverted Data Output	50	Tx7p	Transmitter Non-Inverted Data Input
21	GND	Ground	51	GND	Ground
22	Rx5n	Receiver Inverted Data Output	52	Tx5n	Transmitter Inverted Data Input
23	Rx5p	Receiver Non-Inverted Data Output	53	Tx5p	Transmitter Non-Inverted Data Input
24	GND	Ground	54	GND	Ground
25	Rx3n	Receiver Inverted Data Output	55	Tx3n	Transmitter Inverted Data Input
26	Rx3p	Receiver Non-Inverted Data Output	56	Tx3p	Transmitter Non-Inverted Data Input
27	GND	Ground	57	GND	Ground
28	Rx1n	Receiver Inverted Data Output	58	Tx1n	Transmitter Inverted Data Input
29	Rx1p	Receiver Non-Inverted Data Output	59	Tx1p	Transmitter Non-Inverted Data Input
30	GND	Ground	60	GND	Ground

OSFP Module Pad Layout

Top Side (viewed from top)



Bottom Side (viewed from bottom)



----- Module Card Edge -----

The Active Optical Cable (AOC) pin assignment is SFF-8679 compliant.

Control Signals (OSFP)

The transceivers are CMIS 4.0 compliant, management interface and OSFP 4.1 compliant form factor and interfaces. The control signals shown in the pad layout are implemented with the following functions:

Name	Function	Description
LPWn/PRSn	Input/output	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification.

Name	Function	Description
INT/RSTn	Input,/output	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in the OSFP Specification.
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	Bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.

Diagnostics and Other Features

Note

This document describes hardware features and capabilities. For detailed features availability, contact your NVIDIA representative for [NVIDIA Support](#) for the firmware release notes.

The transceiver has a microcontroller with functions for monitoring supply voltage, temperature, laser bias current, optical transmit and receive levels with associated warning and alarm thresholds that can be read by the switch software and viewed remotely.

The transceiver supports the following key features from the OSFP MSA specification:

1. Physical layer link optimization.
2. Digital Diagnostic Monitoring (DDM).
3. Page 13h and 14h Module Diagnostics
4. Interrupt indications.

Other CMIS functions, such as FW upgrade, are supported via CDB commands.

Specifications

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-40	85	°C
Operating Case Temperature	T_{OP}	0	70	°C
Supply Voltage	V _{CC}	-0.5	3.6	V
Relative Humidity (non-condensing)	RH – Option 1	5	65	%
Control Input Voltage	V _I	-0.3	V _{CC} +0.5	V

Note

Maximum switch ambient temperature for reverse (front to back) airflow on QM9700 is 40°C with all fans, and 35°C in case of fan failure.

Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V
Instantaneous peak current at hot plug	ICC_IP	-	-	6800	mA

Parameter	Symbol	Min	Typ	Max	Units
Sustained peak current at hot plug	ICC_SP	-	-	5670	mA
Maximum Power Dissipation	PD	-	16	17	W
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	1.5	W
Signaling Rate per Lane	SRL	-	53.125	-	GBd
Two Wire Serial Interface Clock Rate	-	100	-	1000	kHz
Power Supply Noise Tolerance (10Hz - 10MHz)	-	-	-	25	mV
Rx Differential Data Output Load	-	-	100	-	Ohm
Operating Distance	-	2	-	(OPN dependent)	m

Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Units
Receiver (Module Output)					
Peak-peak AC common-mode voltage	VCMLF	17	-	32	mV
	VCMFB	-	-	80	
Differential output Voltage (Long mode)		-	-	900	mV
Differential output Voltage (Short mode)		-	-	600	mV
Eye height, differential		15	-	-	mV
Differential Termination Mismatch		-	-	10	%
Transition Time (min, 20% to 80%)		8.5	-	-	ps
DC common mode Voltage		-350	-	2850	mV
Transmitter (Module Input)					
Differential pk-pk input Voltage tolerance		750	-	-	mV
Differential termination mismatch		-	-	10	%
Single-ended voltage tolerance range		-0.4	-	3.3	V
DC common mode Voltage		-350	-	2850	mV

Notes:

Amplitude customization beyond these specs is dependent on validation in customer system.

Electrical Specification for Low Speed Signal

Parameter	Symbol	Min	Max	Units
Module output SCL and SDA	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V

Optical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Wavelength	$\lambda 1/\lambda 5$	1264.5	1271	1277.5	nm	
	$\lambda 2/\lambda 6$	1284.5	1291	1297.5		
	$\lambda 3/\lambda 7$	1304.5	1311	1317.5		
	$\lambda 4/\lambda 8$	1324.5	1331	1337.5		
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each lane	AOPL	-3.2	-	4.4	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each lane min: <ul style="list-style-type: none"> for TDECQ < 1.4 dB for 1.4 dB ≤ TDECQ ≤ 3.4 dB 	TOMA	-0.2 -1.6 + TDECQ	-	3.7	dBm	2
TDECQ minus TECQ, each lane	TDECQ-TECQ	-	-	2.5	dB	

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-16	dBm	
Extinction Ratio, each lane	ER	3.5	-	-	dB	
RIN _{21.4OMA}	RIN	-	-	-136	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	17.1	dB	
Transmitter Reflectance	TR	-	-	-26	dB	3
Receiver						
Wavelength	λ_1/λ_5	1264.5	1271	1277.5	nm	
	λ_2/λ_6	1284.5	1291	1297.5		
	λ_3/λ_7	1304.5	1311	1317.5		
	λ_4/λ_8	1324.5	1331	1337.5		
Damage Threshold, average optical power, each lane	AOPD	4.5	-	-	dBm	
Average Receive Power, each lane	AOPR	-7.2	-	4.4	dBm	
Receive Power (OMA _{outer}), each lane	OMA-R	-	-	3.7	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMA _{outer}), each lane	SOMA	-	-	-4.6	dBm	4
Stressed Receiver Sensitivity (OMA _{outer}), each lane	SRS	-	-	-2.6	dBm	5
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ)			3.4		dB	
OMA _{outer} of each aggressor lane			1.5		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if TDECQ < 1.4dB, OMA_{outer} (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.
4. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
5. Measured with conformance test signal at TP3 for the BER = 2.4x10⁻⁴

Connector Details

Single-mode Duplex LC PC to Duplex LC PC Optical Connector

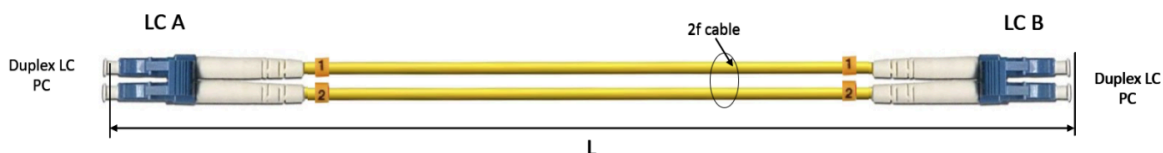
The fiber which connects connector A lane 1 must end at connector B lane 2 at the other end of the link.

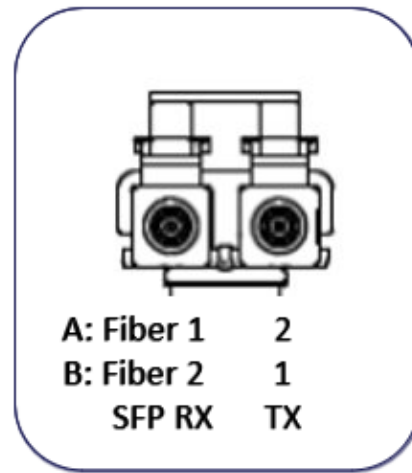
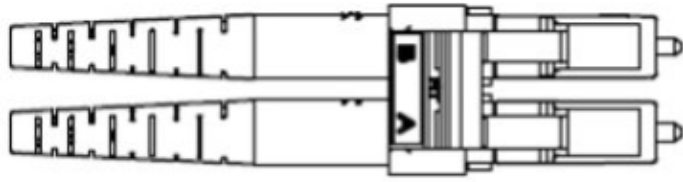
Duplex LC to Duplex LC Patch Cable Fiber Connections:

Connector A Duplex LC	Connection	Connector B Duplex LC
1	----->	2
2	<-----	1

Multiple Duplex LC patch cables can be connected in series, but each added connector pair adds reflections in the link which impairs performance.

Typical Single Mode Duplex LC Fiber Patch Cable:





Mechanical Specifications

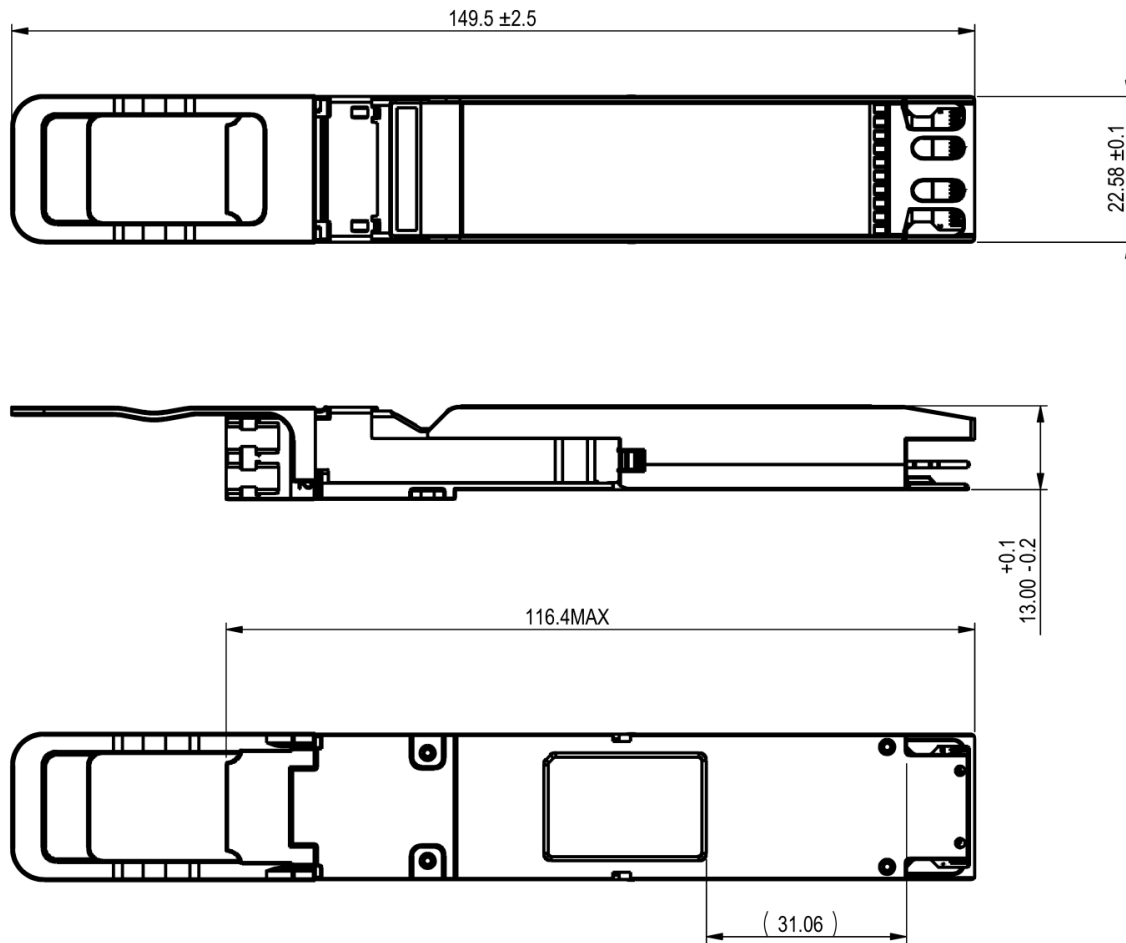
(i) Note

Shipped packages may vary in size, artwork, raw materials and other packaging elements.

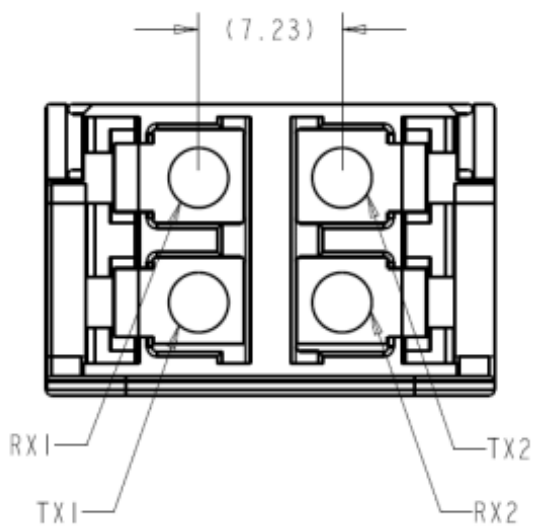
(i) Note

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Option 1



Connector



Labels

Back shell Label

The label applied on the transceiver's back-shell is illustrated below. Note that the Images are for illustration purposes only. Labels look and placement may vary.

Transceiver Label (Illustration)



i Note

Images are for illustration purposes only. Product labels, colors, and form may vary.

Transceiver Back-Shell Label Serial Number Legend

Symbol	Meaning	Notes
MT	Manufacturer name (Mellanox Technologies)	2 digits (alphanumeric)
YY	Year of manufacturing	2 last digits of the year (numeric)
WW	Week of manufacturing	2 digits (numeric)

JC <i>or</i> DM	Manufacturer Site: JC – Option 1 (China) DM – Option 2 (Malaysia)	Two characters
SSSSS	Serial number	5 digits (decimal numeric) for serial number, starting from 00001.

Regulatory Compliance

The transceiver is a Class 1 laser product. It is certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50
Electrical Safety	CB	IEC 62368
Electrical Safety	UL/CSA	UL 62368 and CAN/CSAN 62368

Handling and Cleaning

The transceiver can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Observe normal handling precautions for electrostatic discharge-sensitive devices.

The transceiver is shipped with dust caps on both the electrical and the optical port. The cap on the optical port should always be in place when there is no fiber cable connected. The optical connector has a recessed connector surface which is exposed whenever it has no cable nor cap.

Important note 1: Keep both the fiber and transceiver dust caps.

Important note 2: Clean both transceiver receptacle and cable connector prior to insertion of the fiber cable, to prevent contamination from it.

The dust cap ensures that the optics remain clean during transportation. Standard cleaning tools and methods should be used during installation and service. Liquids must not be applied.

Important note 3: 80% of transceiver link problems are related to dirty optical connectors.

Part Numbers and Description

Legacy PN	Ordering PN	Description
MMS4X90-NR	980-9IB70-00YL00	NVIDIA twin port transceiver, 800Gbps, 2xLR4, OSFP, 2xLC-LC, 1310nm SMF, up to 10km, finned

Document Revision History

Rev	Date	Description
1.0	Apr. 2026	Initial release.

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